

TENTATIVE COURSE OUTLINE

WK	TOPICS	ACTIVITIES
1	F 9/3: Introduction and Review	Read: Chapter 1, 2.1
2	M 9/6: NO CLASS (Labor Day) W 9/8: Boolean Algebra F 9/10: Boolean Algebra, Fundamental Exam (1st attempt)	Read: 2.2-2.3 Fundamental Exam (In Class) F 9/10
3	M 9/13: K-Maps W 9/15: More K-Maps, Prime Implicants F 9/17: High-Impedance Gates, Universal Gates	Read: 1.6, 2.4-2.10 Written HW #1 Due Th 9/16 A: Pre #1 Due W 9/15
4	M 9/20: Common Combinational Structures W 9/22: Digital Logic with Combinational Structures F 9/24: Adders, Complements, Subtractors	Read: 3.5-3.9, 4.1-4.4 Written HW #2 Due Th 9/23 A: Demo #1 B: Pre #1 Due W 9/22
5	M 9/27: Carry-Lookahead Adders W 9/29: Specialized Arithmetic Structures F 10/1: Arithmetic Logic Units	Read: "CLAs", 4.5, 9.3 A: Post #1, Pre #2 Due W 9/29 B: Demo #1
6	M 10/4: D Latches and FFs, FF Timing W 10/6: Intro to Sequential Circuits, Counters F 10/8: Sequential Circuit Analysis and Design	Read: "D Latch and FF", 5.4-5.5 Written HW #3 Due Th 10/7 A: Demo #2 B: Post #1, Pre #2 Due W 10/6
7	M 10/11: Midterm #1 Review (Optional) W 10/13: Seq. Circuit Timing, Asynchronous Issues F 10/15: FSMs and Sequential Circuit Design	MIDTERM #1 Read: 6.1-6.7, "Sequential Timing" A: Post #2 Due W 10/13 B: Demo #2
8	M 10/18: FSMs and Sequential Circuit Design W 10/20: NO CLASS F 10/22: NO CLASS	Read: 5.7 Written HW #4 Due Th 10/21 A: Pre #3 Due W 10/20 B: Post #2 Due W 10/20
9	M 10/25: FSM Implementation W 10/27: Other FF Types and FSMs F 10/29: Design Examples	Read: 5.6 A: Demo #3 B: Pre #3 Due W 10/27
10	M 11/1: NO CLASS W 11/3: Registers, Register Transfers, Micro-operations F 11/5: Complex FSM Design w/Registers	Read: 7.1-7.3, 7.5-7.8 Written HW #5 Due Th 11/11 A: Post #3, Pre #4 Due W 11/3 B: Demo #3
11	M 11/8: NO CLASS W 11/10: NO CLASS F 11/12: Complex FSMs Design w/Registers, Datapath/Control	Read: 7.10 A: Demo #4 B: Post #3, Pre #4 Due W 11/10
12	F 11/15: Building Datapaths F 11/17: Designing Control M 11/19: Design Examples	Read: 9.1-9.6 Written HW #6 Due Th 11/18 A: Post #4 B: Demo #4
13	M 11/23: Midterm #2 Review (optional) W 11/25: NO CLASS F 11/27: NO CLASS (Thanksgiving)	MIDTERM #2 B: Post #4 Due T 11/24
14	M 11/29: SRAM and DRAM W 12/1: Designing SRAM F 12/3: SRAM Arrays	Read: 8.1-8.4 "SRAM Arrays" Written HW #7 Due Th 12/2 A: Pre #5 Due Th 12/2 B: Pre #5 Due Th 12/2
15	M 12/6: Processor Design W 12/8: Circuit Pipelining, Serial Transfers F 12/10: NO CLASS	Read: 9.7-9.8, 10.1 A: Demo #5 ** B: Demo #5 **
16	M 12/13: NO CLASS W 12/15: Final Exam Review (Optional) F 12/17: NO CLASS (classes finished 12/15)	Written HW #8 Due T 12/12 A: Post #5 Due W 12/15 B: Post #5 Due W 12/15
FINAL EXAM – Sunday 12/19 @ 7:25pm		