## COURSE OBJECTIVES (UPDATED 03/15)

### Library Delay Modeling
- Define propagation delay, slew/transition time.
- Define timing arcs, unateness.
- Show how unateness concept is incorporated for static timing analysis.
- Understand the NLDM (nonlinear delay modeling) form for cell delay modeling.
- List the required parameters for extracting cell delay from library.
- For a given cell description in NLDM form, answer timing-related questions.
- Explain state-dependent modeling with an example.
- Show extrapolating cell delay if no exact entry in lookup table.

### Clock Synthesis
- Define clock parameters.
- List causes of uncertainty in clock network parameters.
- Explain clock network synthesis objectives.
- Explain the impact of clock parameters on clock synthesis objectives.
- Explain different clock topologies, their pros and cons.
- Write setup/hold checks in an example circuit.
- Write setup/hold checks in generic case.
- Explain the steps in clock tree synthesis.
- Explain high-level idea of MMM algorithm for clock tree topology generation.
- Modeling a given interconnect as distributed RC.
- Compute delay of an interconnect tree using the Elmore model.
- Explain all the steps in the zero-skew algorithm (Tsay 1993).
- Solve example on tapping point computation in the Tsay algorithm.
- Explain need for applying the snaking technique.
- Explain all the steps in the DME algorithm (Kahng 1993).
- Explain the benefits of defining merging segments and tiled rectangular region.

### Retiming and Clock Skew Scheduling
- Write clock skew scheduling formulation for long and short paths in the circuit.
- Write setup/hold checks for all types of design paths (IN/FF, FF/FF, FF/OUT).
- Combine a range of clock skew to be passed to clock synthesis stage.
- Understand the basic retiming equation.
- Apply forward and backward retiming at a node for the general case.
- Apply the same for special cases (different FF types, set/reset conditions).
- Formulate an instance of retiming problem as ILP for min-delay and min-area.
- Apply steps yielding to min-delay formulation (e.g. computing weight and delay matrixes).

### Crosstalk
- Define different types of capacitances of a route in a multi-layer design.
- Explain the impact of technology scaling on different capacitance types.
- Explain different types of crosstalk-induced noise.
- Explain all factors impacting crosstalk-induced noise.
- Modeling parallel and coupled RC lines with equivalent capacitance.
- Compute equivalent coupling capacitance using Miller factor.
[3] Explain the need for pruning in crosstalk analysis.
[1] Explain an effective order for applying different types of pruning.
[2] List a number of crosstalk prevention mechanisms.
[2] List a number of techniques for fixing a detected crosstalk-induced noise.
[2] Ability to list possible pros or cons of using a crosstalk noise repair mechanism.
[2] Incorporate provided (new) logic exclusivity constraint in the ILP.