

AMIN FARMAHINI-FARAHANI

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EDUCATION AND ACADEMIC RESEARCH

Ph.D. Candidate in Computer Engineering

Madison Embedded Systems and Architectures Lab., Department of Electrical and Computer Engineering, University of Wisconsin-Madison, WI, Expected 2013

Advisor: Prof. Michael J. Schulte

Research Assistantship: *FPGA-based Design for the CERN Large Hadron Collider*

- Contribution to design and implementation of the CERN Clustering Algorithm on FPGA
- Hardware and software development for the FPGA-based Auxiliary Card including RocketIO, S-link, TTC, and TTS ports; used in the next generation of Compact Muon Solenoid (CMS) trigger
- Development and implementation of flexible, low-latency sorting units on FPGA for the CMS trigger upgrade

M.Sc. in Computer Architecture Design

Silicon Intelligence and VLSI Signal Processing Lab., School of Electrical and Computer Engineering, University of Tehran, Tehran, Iran, Feb. 2008

Advisors: Prof. Sied Mehdi Fakhraie and Prof. Saeed Safari

GPA: 19.52 out of 20 (Rank 1st)

Thesis: *Design and Implementation of Bio-Inspired Hardware Cores*

- Design and implementation of a pipelined core for performing particle swarm optimization (PSO) processes on FPGA
- Development and implementation of an on-chip multi-processing architecture for PSO algorithm computations based on an SOPC platform
- Presenting a method for hardware implementation of PSO algorithm for computational intensive applications based on mesh architecture
- Design and implementation of a reconfigurable approach for on-chip feedforward neural network training through PSO algorithm

B.Sc. in Computer Hardware Engineering

Information Technology Research Center, Department of Computer Engineering, Iran University of Science and Technology (IUST), Tehran, Iran, June 2005

Advisor: Prof. Mohammad Reza Jahed-Motlagh

GPA: 17.23 out of 20 (Rank 1st)

Thesis: *Combinational Circuits Design using Evolutionary Algorithms*

- Developing a software framework for extrinsic evolution of combinational circuits using genetic algorithm and particle swarm optimization algorithm

RESEARCH INTERESTS

- Reconfigurable Computing and FPGA Design
- Embedded Systems Design and HW/SW Codesign
- Bio-Inspired and Intelligent Systems Computing
- System-On-a-Chip (SOC) Design and On-Chip Multiprocessing (CMP)
- Computer Architecture and On-Chip Networks
- Application Specific Hardware Cores

GRADUATE- LEVEL COURSES

- Embedded Computing
- Multiprocessor Architecture
- Advanced Computer Architecture
- ASIC Design
- VLSI Systems Design
- Digital System Design with VHDL
- Digital Systems Testing and Design for Testability
- Low-Power Integrated Circuit Design
- Bio-Inspired Computing
- Parallel Processing
- Design Validation and Verification

PROFESSIONAL EXPERIENCE

Research

- Graduate Research Assistant, *Madison Embedded Systems and Architectures Lab.*, Department of Electrical and Computer Engineering, University of Wisconsin-Madison, WI, Sep. 2008 to present
- Research Assistant (RFID in Automotive Industry), *Research Institute of Advanced Technologies in Automotive Industry*, University of Tehran, Tehran, Iran, May 2006 to Mar. 2008
- Graduate Research Assistant, *Silicon Intelligence and VLSI Signal Processing Lab.*, Electrical and Computer Engineering Department, University of Tehran, Tehran, Iran, Sep. 2005 to Feb. 2008
- Research Assistant (VoIP), *Information Technology Research Center*, Department of Computer Engineering, Iran University of Science and Technology, Tehran, Iran, June 2003 to June 2005
- Intern (Wireless Personal Area Network), *Microelectronic Research and Development Center of Iran (MERDCI)*, Tehran, Iran, Summer 2004

Teaching

- **Instructor**, Department of Computer Engineering, Iran University of Science and Technology, Tehran, Iran
 - *Undergraduate-Level Course, Digital Logic Circuits Laboratory*, Spring and Summer 2007
 - *Undergraduate-Level Course, Digital Electronics Laboratory*, Summer 2007
- **Teaching Assistant**, School of Electrical and Computer Engineering, University of Tehran, Tehran, Iran
 - *Graduate-Level Course, ECE 365: Advanced VLSI*, Fall 2006
 - *Senior-Level Course, ECE 446: VLSI System Design*, Fall 2006
- **Teaching Assistant**, Department of Computer Engineering, Iran University of Science and Technology, Tehran, Iran
 - *Undergraduate-Level Course, Digital Logic Circuits*, Fall 2004 to present (seven Semesters)
 - *Undergraduate-Level Course, Computer Architecture*, Spring 2005 to Spring 2006

Reviewer

- Reviewer for IEEE International Conference on Intelligent & Advanced Systems, 2007

PROFESSIONAL SKILLS

Hardware Description Languages

Verilog, VHDL, Verilog PLI

EDA Tools

Altera Quartus II, Nios II Embedded Design Suite, Altera SOPC Builder, Aldec Active HDL, Electronics Workbench, HSPICE, LeonardoSpectrum, ModelSim, Synplify Pro, Tanner L-Edit, Xilinx ISE, Xilinx Embedded Development Kit and Platform Studio, Xilinx CORE Generator, Cadence Virtuoso, Cadence SOC Encounter, CodeComposer Studio, OrCAD (some), Xilinx ChipScope Pro (some)

Programming Languages and Libraries

Pascal, Z-80 & MIPS assembly, C/C++, MPI parallel processing library, HTML, ASP (some)

Application and General Computer Software

MATLAB (some), LaTeX, DOS, Windows 98/ME/2000/XP, Linux, Microsoft Office, Visio, FrontPage, Visual Studio

AWARDS AND HONORS

- ECE Wisconsin Distinguished Graduate Fellowship, 2008
- Annual University of Tehran Top Students Award, 2008
- Ranked 1st among 14 Computer Engineering (Computer Architecture Design) graduate students at the University of Tehran, 2008
- Ranked 18th in the Iranian Nationwide Computer Engineering M.Sc. Entrance Exam in hardware major among more than 10,000 participants, 2005
- Ranked 1st (Top Student) among more than 90 Computer Engineering undergraduate students at Iran University of Science and Technology, 2005
- Annual Iran University of Science and Technology Top Students Award, 2004 and 2005

MEMBERSHIP

IEEE Student Member, Jan. 2007 to present
Member of Iranian Elite Foundation, May 2008 to present

PUBLICATION

Published Journal Papers

1. **A. Farmahini-Farahani**, S. Vakili, S. M. Fakhraie, S. Safari, and C. Lucas, "Parallel Scalable Hardware Implementation of Asynchronous Discrete Particle Swarm Optimization," Accepted for Publication in *Elsevier J. of Engineering Applications of Artificial Intelligence*.
2. M. Ghaffari-Miab, **A. Farmahini-Farahani**, R. Faraji-Dana, and C. Lucas, "An Efficient Hybrid Swarm Intelligence-Gradient Optimization Method for Complex Time Green's Functions of Multilayer Media," *Progress in Electromagnetics Research (PIER)*, vol. 77, pp. 181-192, 2007.

Conference Papers

1. **A. Farmahini-Farahani**, C. Tsen, and K. Compton, "FPGA Implementation of a 64-Bit BID-Based Decimal Floating-Point Adder/Subtractor," in *Proc. IEEE Intl. Conf. on Field-Programmable Technology (FPT)*, Sydney, Australia, Dec 2009.
2. A. Gregerson, **A. Farmahini-Farahani**, W. Plishker, Z. Xie, K. Compton, S. Bhattacharyya, and M. Schulte, "Advances in Architectures and Tools for FPGAs and their Impact on the Design of Complex Systems for Particle Physics," in *Typical Workshop on Electronics for Particle Physics (TWEPP)*, Sep. 2009, Paris, France.
3. A. Gregerson, **A. Farmahini-Farahani**, B. Buchli, S. Naumov, M. Bachtis, K. Compton, M. Schulte, W. Smith, and S. Dasu, "FPGA Design Analysis of the Clustering Algorithm for the CERN Large Hadron Collider," in *Proc. IEEE Intl. Symp. on Field-Programmable Custom Computing Machines (FCCM)*, Napa, CA, Apr. 2009, pp. 19-26.
4. **A. Farmahini-Farahani**, S. M. Fakhraie, and S. Safari, "Scalable Architecture for on-Chip Neural Network Training using Swarm Intelligence," in *Proc. of the Design, Automation and Test in Europe Conf. (DATE)*, Munich, Germany, Mar. 2008, pp. 1340-1345.
5. **A. Farmahini-Farahani**, S. M. Fakhraie, and S. Safari, "SOPC-Based Architecture for Discrete Particle Swarm Optimization," in *Proc. IEEE Intl. Conf. on Electronics,*

- Circuits and Systems (ICECS)*, Marrakech, Morocco, Dec. 2007, pp. 1003-1006.
6. N. Sedaghati-Mokhtari, M. N. Bojnordi, **A. Farmahini-Farahani**, M. Mousavinezhad, and S. M. Fakhraie, "Simulation of Voice Processing Applications through VLIW DSP Architectures," in *Proc. IEEE Intl. Conf. on Electronics, Circuits and Systems (ICECS)*, Marrakech, Morocco, Dec. 2007, pp. 291-293.
 7. **A. Farmahini-Farahani**, M. Laali, A. Moghimi, S. M. Fakhraie, and S. Safari, "Mesh Architecture for Hardware Implementation of Particle Swarm Optimization," in *Proc. IEEE Intl. Conf. on Intelligent & Advanced Systems (ICIAS)*, Kuala Lumpur, Malaysia, Nov. 2007, pp. 1300-1305.
 8. A. Naghdinezhad, **A. Farmahini-Farahani**, M. R. Hashemi, and O. Fatemi, "An Adaptive Unequal Error Protection Method for Error Resilient Scalable Video Coding using Particle Swarm," in *Proc. IEEE Intl. Conf. on Signal Processing and Communication (ICSPC)*, Dubai, UAE, Nov. 2007, pp. 396-399.
 9. H. Assasi, **A. Farmahini-Farahani**, M. Hamzeh, S. Mohammadi, and C. Lucas, "Input Stimuli Evolution for RFID Tag Functional Verification," in *Proc. IEEE Intl. Conf. on RFID Eurasia*, Istanbul, Turkey, Sep. 2007, pp. 1-6.
 10. **A. Farmahini-Farahani**, M. Kamal, S. M. Fakhraie, and S. Safari, "HW/SW Partitioning using Discrete Particle Swarm," in *Proc. ACM Great Lakes Symp. on VLSI (GLSVLSI)*, Stresa-Lago Maggiore, Italy, Mar. 2007, pp. 359-364.
 11. **A. Farmahini-Farahani** and S. M. Fakhraie, "SOPC-Based Particle Swarm Optimization," in *Proc. Intl. CSI Computer Conf.*, Tehran, Iran, Feb. 2007, pp. 1536-1541.
 12. M. H. Neishabouri, M. Hamzeh, **A. Farmahini-Farahani**, P. Saeedi, M. Daneshtalab, and N. Yazdani, "Voltage Scheduling Technique during System Level Design Using UML-RT Model," in *Proc. IEEE Design and Test Workshop*, Dubai, UAE, Nov. 2006.
 13. P. Saeedi, **A. Farmahini-Farahani**, M. Hamzeh, M. H. Neishabouri, and A. Afzali-Kusha, "Network-On-Chip Thermal-Balanced Mapping," in *Proc. IEEE Design and Test Workshop*, Dubai, UAE, Nov. 2006.
 14. **A. Farmahini-Farahani**, M. Kamal, and M. Salmani-Jelodar, "Parallel-genetic-algorithm-based HW/SW Partitioning," in *Proc. IEEE Intl. Symp. on Parallel Computing in Electrical Engineering (PARELEC)*, Bialystok, Poland, Sep. 2006, pp. 337-342.
 15. M. Kamal, **A. Farmahini-Farahani**, and M. Salmani-Jelodar, "Automatic Combinational Circuit Design using Genetic Algorithm," in *Proc. Conf. Intelligent Systems*, Tehran, Iran, 2005 (Persian).

REFERENCES

Prof. Michael J. Schulte, University of Wisconsin-Madison: schulte@engr.wisc.edu
 Prof. Katherine Compton, University of Wisconsin-Madison: kati@engr.wisc.edu
 Prof. Sied Mehdi Fakhraie, University of Tehran: fakhraie@ut.ac.ir
 Prof. Saeed Safari, University of Tehran: saeed@ut.ac.ir
 Prof. Caro Lucas, University of Tehran: lucas@ipm.ir
 Prof. M. R. Jahed-Motlagh, Iran University of Science and Technology: jahedmr@iust.ac.ir