1. (15 Points) Register Transfers, bus

1. (8 points) The following register transfer operations will be implemented where $K1, K0$ are two input Boolean variables:

- $\overline{K1} \cdot K0$: $R1 \leftarrow R2$
- $K1 \cdot K0$: $R2 \leftarrow R3$
- $K1 \cdot K0$: $R3 \leftarrow R2$
- $K1 \cdot K0$: $R1 \leftarrow R4$

All four $n$-bit registers $R1, R2, R3,$ and $R4$ have three-state bi-directional input/output lines connecting to a single shared bus as shown in the figure below. Fill in the control signals (Load and En(able)) to each of these four registers so that the above conditional register transfer operations can be realized.

**Answer:**

<table>
<thead>
<tr>
<th></th>
<th>Load</th>
<th>EN</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>$\overline{K1} \cdot K0 + K1 \cdot K0$</td>
<td>0</td>
</tr>
<tr>
<td>R2</td>
<td>$\overline{K1} \cdot K0$</td>
<td>$K0$</td>
</tr>
<tr>
<td>R3</td>
<td>$K1 \cdot \overline{K0}$</td>
<td>$\overline{K1} \cdot K0$</td>
</tr>
<tr>
<td>R4</td>
<td>0</td>
<td>$K1 \cdot K0$</td>
</tr>
</tbody>
</table>
2. (7 points) The following is a list of register transfer micro-operations. They are originally written so that they can be executed from top to bottom in a sequential order.

\[
\begin{align*}
R2 & \leftarrow R1 \\
R3 & \leftarrow R5 \\
R4 & \leftarrow R1 \\
R1 & \leftarrow R5 \\
R5 & \leftarrow R6
\end{align*}
\]

In order to accelerate computation, it is possible to execute more than one micro-operations per clock cycle without altering the final results in each register. Consider two situations:

(i) (4 points) Suppose that each register is connected to a single three-state bus via bi-directional input/output lines. Execute above five micro-operations in no more than three clock cycles:

**Answer:**

\[
\begin{align*}
R2 & \leftarrow R1; R4 \leftarrow R1 \\
R3 & \leftarrow R5; R1 \leftarrow R5 \\
R5 & \leftarrow R6
\end{align*}
\]

(ii) (3 points) Suppose that the number of buses has no limit. Can all these micro-operations be implemented within a single clock cycle? Give explanation to your answer.

[ ] YES [ ] NO

**Explanation:** With 3 buses, R1, R5, and R6 can place their content onto a bus each to be loaded by other registers.
2. (10 points) ALU

Depicted above is an ALU bit slice which can perform both arithmetic and logic operations by choosing appropriate control signals $C_{in}, S_0$ and $S_1$. When $i = 0$, $C_i = C_{in}$. Let $F = F_{n-1}...F_1F_0$ to be the output, $A = A_{n-1}...A_1A_0$ and $B = B_{n-1}...B_1B_0$. Complete the function table below.

**Answer:**

<table>
<thead>
<tr>
<th>$S_1$</th>
<th>$S_0$</th>
<th>$C_{in} = 0$</th>
<th>$C_{in} = 1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>$A \oplus B$</td>
<td>$A$</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>$\overline{A}$</td>
<td>$A \oplus B$</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>$A + B$</td>
<td>$A + I$</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>$A - I$</td>
<td>$A - B$</td>
</tr>
</tbody>
</table>