Last (Family) Name: _________________________
First (Given) Name: _________________________
Student ID: _________________________________

Instructor: (circle one)  RAMANATHAN  DIETMEYER

ECE/Comp. Sci. 352 – Digital System Fundamentals

Quiz # 4
Thursday, December 2, 1999

- Closed Book Examination
- Duration: 75 minutes
- Double check your answers. Only completely correct answers will receive full credit. Partial credit will be given conservatively.
- Please write your name on all pages.
- Illegible writing and drawings will not receive any credit, even if you believe them to express the correct answer.

<table>
<thead>
<tr>
<th>Problem</th>
<th>Points</th>
<th>Score</th>
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<tbody>
<tr>
<td>1</td>
<td>20</td>
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<td>2</td>
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<td>Total</td>
<td>100</td>
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</table>
1. (20 points) Design a 4-bit shift register that performs the following operations based on the 2-bit control input SC(1:0).

<table>
<thead>
<tr>
<th>SC(1:0)</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>No shift</td>
</tr>
<tr>
<td>0 1</td>
<td>Shift right (down), fill in 0</td>
</tr>
<tr>
<td>1 0</td>
<td>Shift right (down), fill in with sign bit. Assume number in the register is in 2’s-complement representation.</td>
</tr>
<tr>
<td>1 1</td>
<td>No shift</td>
</tr>
</tbody>
</table>

Neatly draw your design using the flip-flops given below. On the left of the page draw logic that serves all cells, if any is needed.
2. (20 points) Design a synchronous circuit with two periodic outputs $P_1$ and $P_2$ satisfying the following timing relationship to the clock (Clk). Assume $P_1$ and $P_2$ have a period of 40ns and the Clk has a period of 10ns.

Use only positive edge-triggered JK flip-flops and logic gates in your design. If your design must be initialized to a certain starting state, show the wiring and input signal necessary to achieve this initialization. Draw your design neatly; we must be able to follow all of the wiring.

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**Binary Counter plus Decoder**

**Ring Counter: Only one FF must be set**

**Self-Starting Ring Counter**

**Twisted Ring Counter**
3. A combinational circuit is a direct realization of the switching function: 
   \[ f = \overline{ac} + ad + a\overline{b} \]

   The circuit is a two-level AND-OR circuit with inverters at the input to generate \( \overline{a} \) and \( \overline{b} \). All gates and inverters have a delay of 1ns.

   (a) **(6 points)** Can a single input change cause a static-1 hazard in this circuit? If yes, identify a single input change that causes a static-1 hazard. Use a Karnaugh map to demonstrate the static-1 hazard you have identified.

   Yes *(cross one out)*

   ![Karnaugh Map](image)

(b) **(7 points)** Can a two input change cause a 0-functional hazard in this circuit? If yes, identify a two input change that causes a 0-functional hazard. Use a Karnaugh map to demonstrate the 0-functional hazard you have identified.

   Yes

   ![Karnaugh Map](image)

(c) **(7 points)** What additional gates must be included in this circuit to eliminate all static-1 hazards without changing its function (obviously). Show the additional gates on a Karnaugh map instead of drawing a logic diagram.

   ![Karnaugh Map](image)
4. The figure shows a 64K×8 memory system. Assumes the lines not shown have been connected properly; they are not relevant for answering the questions below.

(a) (5 points) Which memory chips (identified by M0, M1, ..., M7) contain the address 08500H?

0 1000 0101 0000 0000 lies in M4 and M5.
M0 and M1 contain the first 16K addresses (00000H to 03FFFH). M2 and M3 contain the addresses from 16K to 32K (04000H to 07FFFH). M4 and M5 contain the addresses from 32K to 48K (08000H to 0BFFFH). M6 and M7 contain the addresses from 48K to 64K (0C000H to 0FFFFH).

(b) (10 points) Suppose you want to increase the memory size to 96K×8 by adding a 32K×8 RAM IC. Augment the figure to show the decoding logic and the address lines to the new IC. You need not show the data lines, Read, and Write lines. If necessary, you may use additional gates.

(c) (5 points) Within a memory chip what is the advantage of using a row and column decoder as opposed to a single decoder? Limit your answer to a sentence or two.

The row and column decoders are much smaller than what will be required in a single decoder scheme. Smaller decoders are usually faster, thereby increasing the RAM access time.
5. (20 points) Show the programming to implement a full adder using the \half{} of a 10L8 PAL shown below. Put a clear \times{} where each connection is to be made, and only at those cross-points. Recall that, \sum{} and \cout{} of a full adder are:

\[
\begin{align*}
\text{SUM} & = A \oplus B \oplus \cin \\
\text{Cout} & = A \cdot B + (A \oplus B) \cdot \cin
\end{align*}
\]

Use the minimum number of PAL outputs. Some inputs and outputs have been labeled. If you use additional outputs label them with the logic function that they implement. (If a used PAL output is not labeled you will not get any credit for this question even if your answer is fully correct.) If external wiring to connect an output to an input is needed, draw that wiring with your straight-edge.

Slightly more expensive solutions include generating

\[
\overline{\text{Cout}} = A \cdot B + (A \oplus B) \cdot \cin
\]

and then using an additional PAL as an inverter.