1. *(Register) Problem 5.3 in text book.

2. *(Register transfer) Problem 5.6 in text book.

3. (Serial subtracter) Problem 5.7 in text book.
   The SO output to register B must be inverted and the initial carry must be 1, this forms the 2’s complement of the contents of register B. If A less than B, the final value left in the carry flip flop will be 0. If A greater than B, then the result will be the 2’s complement form.

4. (Register) Problem 5.8 in text book.
   Answer:

5. *(Ring counter) Problem 5.10 in text book.

   Solution:
   Since the output of each flip flop is fed as a clock input to the next stage, the delay is propagated.
   The total delay is 16 * 2ns = 32ns
   Maximum Frequency = 1/T = 1/32ns = 31.25 MHz

7. (Counter) Problem 5.14 in text book.
   Answer:
   (a) 01100111 → 01101000 Four flipflops will be complemented
   (b) 00011111 → 00100000 Six flipflops will be complemented


10. (Counter) Problem 5.22 in text book.
   Answer:
   a) 
   b) 

   Answer:  
   \[ JQ8 = Q1Q2Q4, KQ8 = Q1 \]
   \[ JQ4 = Q1Q2, KQ4 = Q1Q2 \]
   \[ JQ2 = Q1Q8, KQ2 = Q1 \]
   \[ JQ1 = 1, KQ1 = 1 \]


   Answer: a) 2 exp 15 b) 2 exp 23 c) 2 exp 27 d) 2 exp 29


15. Additional Problem 1 a) Arrows between pairs: \( \overline{A} \overline{B} \overline{C} \) and \( \overline{A} B \overline{C} \), \( \overline{A} \overline{B} C \) and \( A \overline{B} C \), and \( A B \overline{C} \) and \( A B C \).

   b) Add NAND gates implementing product terms: \( \overline{A} \overline{C} \), \( \overline{B} C \), and \( A B \).

16. Additional Problem 2a)
<table>
<thead>
<tr>
<th>Old $A$ $B$ $C$ $D$</th>
<th>New $A$ $B$ $C$ $D$</th>
<th>Potential hazard types</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 1 0 1</td>
<td>1 1 0 1</td>
<td></td>
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<tr>
<td>1 1 0 1</td>
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<tr>
<td>1 1 0 1</td>
<td>1 1 0 0</td>
<td></td>
</tr>
</tbody>
</table>

(b) Answer: $Y = \overline{AB} + BD + AC \bar{D}$

Static Hazard shown by double arrows

Fixing static Hazard by adding product term $BD$