Homework 2 covers materials in sections 2.5-2.8, Supplement 1, and sections 3.1-3.8. You need NOT turn in the homework. However, you are strongly advised to do it. Short solutions will be posted on the course website home page shortly. We encourage you to work collaboratively with your classmates to the degree that it facilitates your learning.

Problems with a * have a solution available on the Prentice Hall Companion Website Gallery (http://www.prenhall.com/mano).

1. (Essential prime implicants) *Problem 2-19 (a,c) in text.
2. (Simplification) Problem 2-20 (b,c) in text.
3. (Simplification) *Problem 2-22 (a,b) in text.
4. (Simplification) *Problem 2-25 (b,c) in text.
5. (Simplification with NAND gates) Problem 2-27 (b) in text.
6. (Implementation with NAND gates) *Problem 2-28 (a,b) in text.
7. (Implementation with NOR gates) Problem 2-27 (b) in text with NOR gates instead of NAND gates.
8. (Multilevel Implementation with NAND gates) Problem 2-29 (a) in text.
9. (Implementation with NOR gates) *Problem 2-30 (b) in text.
10. (Conversion) Problem 2-32 in text.
11. (Minimum multi-level implementation) Problem 2-33 in text.
12. (XOR) Problem 2-35 in text.
13. (XOR) Problem 2-36 in text.
15. (Combinational Logic Analysis) Problem 3-1 in text.
16. (Combinational Logic Analysis) *Problem 3-3 in text.
17. (Combinational Logic Analysis) Problem 3-4 in text.
18. (Hierarchy) *Problem 3-6 in text.
19. (Decoder) Problem 3-8 in text.
20. (Combinational Logic Design) *Problem 3-11 in text.
22. (Design Using a Decoder) Problem 3-17 in text.
23. (Design with Multiple Decoders) *Problem 3-25 in text.
24. (Design Using a Multiplexer) Problem 3-27 in text.
25. (Design Using a Multiplexer) Problem 3-28 in text.