Homework 3 (Spring 2001)

Homework 3 covers materials in sections 3.8-3.14. You need NOT turn in the homework. However, you are strongly advised to do it. Short solutions will be posted on the course website home page shortly. We encourage you to work collaboratively with your classmates to the degree that it facilitates your learning. The material covered by this homework applies to Quiz #2 on March 8.

Problems with a * have a solution available in the Prentice Hall Companion Website Gallery (http://www.prenhall.com/mano).

1. *(Adder bit) Problem 3-35 in text.
2. *(1’s and 2’s Complement) Problem 3-38 in text.
3. (Unsigned Number Subtraction with 2’s Complement) Problem 3-39 (b,d) in text.
4. *(1’s and 2’s Complement) Problem 3-41 in text.
5. (Signed Number Subtraction) Problem 3-42 (a,d) in text.
6. *(Parallel Adder) Problem 3-45 (b,d,e) in text.
7. (Carry Look-Ahead Adder) A four-bit carry look-ahead adder section has inputs: C_n, A_n+3,n = (A_n+3, A_n+2, A_n+1, A_n), and B_n+3,n = (B_n+3, B_n+2, B_n+1, B_n), and outputs: C_{n+4}, S_{n+3,n} = (S_{n+3}, S_{n+2}, S_{n+1}, S_n). It has internal signals: P = (P_{n+3}, P_{n+2}, P_{n+1}, P_n), G = (G_{n+3}, G_{n+2}, G_{n+1}, G_n), and C_{n+3,n+1} = (C_{n+3}, C_{n+2}, C_{n+1}).
   a. Write the equations for P_i, i = n + 3, n + 2, n + 1, and n using XOR.
   b. Write the equations for G_i, i = n + 3, n + 2, n + 1, and n.
   c. Write the equations for C_i, i = n + 4, n + 3, n + 2, and n + 1 as two-level SOP.
8. (Carry Look-Ahead Adder) For the CLA section in problem 7, A_{n+3,n} = 1110 and B_{n+3,n} = 0011, give the values for P_{n+3,n}, G_{n+3,n}, C_{n+4,n+1}, and S_{n+3,n} as vectors.
9. (Carry Look-Ahead Adder) Suppose that two of the sections in problem 7 are connected together. For the right section, n = 0 and for the left section n = 4. Thus, C_{n+4} = C_4 for the right section is connected to C_n = C_4 for the left section. Assume that each P_i function has 3 gate delays, each G_i function has 2 gate delays, each C_i function has two gate delays, and each S_i function has 3 gate delays. Assuming all input values change at the same time, what is the maximum number of gate delays required to compute the value of S_7?
10. (Comparator) Problem 3-47 in text.
11. *(9’s Complement) Problem 3-49 in text.
12. *(10’s Complement) Problem 3-50 in text.
13. (Unsigned Decimal Subtraction) Problem 3-51 (c,d) in text.
14. *(9’s Complement) Problem 3-52 (a) in text.
15. (BCD adder/subtractor) Problem 3-53 in text.