Problem 7:

(a) $P_i = A_i \oplus B_i, \quad i = n+3, n+2, n+1, n.$
(b) $G_i = A_i \cdot B_i, \quad i = n+3, n+2, n+1, n.$
(c) $C_i = G_{i-1} + P_{i-1} \cdot C_{i-1}, \quad i = n+4, n+3, n+2, n+1.$

So, $C_{n+1} = G_n + P_n \cdot C_n$
$C_{n+2} = G_{n+1} + P_{n+1} \cdot C_{n+1}$
$C_{n+3} = G_{n+2} + P_{n+2} \cdot G_{n+1} + P_{n+1} \cdot P_{n+2} \cdot C_n$
$C_{n+4} = G_{n+3} + P_{n+3} \cdot G_{n+2} + P_{n+2} \cdot G_{n+1} + P_{n+1} \cdot C_n$

Problem 8:

$A_{n+3,n} = 1110$
$B_{n+3,n} = 0011$
$P_{n+3,n} = 1101$
$G_{n+3,n} = 0010$
$C_{n+4,n} = 11100$
$S_{n+3,n} = 0001$

Problem 9:

There are 2 separate blocks of the same CLA module that are connected to each other through the signal, $C_4$. From Problem 7, the following equation is derived:

$C_4 = G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0 + P_3 \cdot P_2 \cdot P_1 \cdot G_0$

Since $P_i$ functions take longer (3 delays) than $G_i$ functions (2 delays), the first level computation for $C_4$ will take 3 delays, waiting for the $P_i$ values. Then the $C_i$ function also takes 2 delays. So it takes $3 + 2 = 5$ gate delays in total to compute $C_4$.

Now, the equation for $S_7 = A_7 \oplus B_7 \oplus C_6$. Since $A_7$ and $B_7$ terms are readily available, $C_6$ has to be analyzed first.

But, $C_6 = G_5 + P_5 \cdot G_4 + P_5 \cdot P_4 \cdot C_4$

In the $C_6$ equation, the slowest term to compute is $C_4$ with 5 gate delays from above. Since it also takes 2 gate delays ($C_i$ function) to compute $C_6$, in total $5 + 2 = 7$ gate delays necessary for the $C_6$ computation.

Going back to the $S_7$ equation, we also need 3 gate delays for $S_i$ function.
Hence, it takes $7 + 3 = 10$ gate delays in total to compute $S_7$.

Problem 10: (3-47) The solution to this was inadvertently omitted from the text solutions. It has now been added there.

Here is an alternative solution that uses only two-level logic. It has not been verified. Using CAFE, the following equation is obtained where the inputs are: $A = \{A,B,C,D\}$ and $B = \{E,F,G,H\}$ and the output is $X$

$$X = -D\cdot E\cdot F\cdot G\cdot H + -C\cdot E\cdot F\cdot G + -C\cdot D\cdot E\cdot F\cdot H + -B\cdot E\cdot F + -B\cdot D\cdot E\cdot G\cdot H +$$
$$ -B\cdot C\cdot E\cdot G + -B\cdot C\cdot D\cdot E\cdot H + -A\cdot E + -A\cdot D\cdot F\cdot G + -A\cdot C\cdot F\cdot G +$$
$$ -A\cdot C\cdot D\cdot F\cdot H + -A\cdot B\cdot F + -A\cdot B\cdot D\cdot G\cdot H + -A\cdot B\cdot C\cdot G + -A\cdot B\cdot C\cdot D\cdot H$$

Problem 15:

Extra logic is added to modify the circuit of BCD adder to handle subtraction as well using 9’s complementer. When Add/Subtract = 0, the circuit functions as BCD adder. It is set to 1 for subtraction.

See the block diagram on next page