Overview of Chapter 6

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  - RAM Bit Slice
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  - Cell Arrays and Coincident Selection
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  - Arrays of Static and Dynamic RAMs
Memory Definitions

Memory Unit - A collection of storage cells together with the necessary circuits to transfer information to and from them.

Memory Organization - the basic architectural structure of memory in terms of how data is accessed.

Random Access Memory (RAM) - a memory unit organized to allow data to be transferred to or from any desired cell or collection of cells.

Memory Address - A collection of binary digits interpreted as a number that refers to a basic memory storage element.

Memory Definitions (Continued)

Memory Data - a collection of binary digits to be stored into or accessed from memory cells. Typical data elements are:

BIT - a single binary digit

BYTE - a collection of eight bits accessed together.

WORD - a collection of binary bits whose size is a typical unit of access for the memory. It is typically a power of two multiple of bytes (e.g., 1 byte, 2 bytes, 4 bytes, 8 bytes, etc.).

Memory Operations -- operations on memory data supported by the memory unit. Typically they are read or write operations over some sized data element (bit, byte, word, etc.).
Memory Organization

- Memory is organized as an indexed array of words. The value of the index for each word is referred to as the memory address.
- Memory is often organized to fit the needs of a particular computer architecture. Here are some historically significant computer architectures and their associated memory organization:
  - Digital Equipment Corporation PDP-8 -- used a 12-bit address to address 4096, 12-bit words.
  - IBM 360 -- used a 24-bit address to address 16,777,216 eight bit bytes, or 4,194,304 32 bit words.
  - Intel 8080 -- (8-bit predecessor to the 8086 and thus to the current Intel processors) used a 16 bit address to address 65,536 eight-bit bytes.

Memory Block Diagram

- A basic memory system is shown here:
  - K Address Lines are decoded to address $2^K$ Words of memory.
  - Each Word is N bits.
  - Read and Write are single control lines defining the simplest memory operation.
Memory Organization (example)

- Example memory contents:
- A memory of 3 address bits, 8 data bits will have:
  - \( k = 3 \) and \( N = 8 \) so \( 2^{*3} = 8 \)
  - Addresses labeled 0 to 7.
  - \( 2^{*3} = 8 \) Words of 8-bit data

<table>
<thead>
<tr>
<th>Memory Address</th>
<th>Memory Content</th>
</tr>
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<tbody>
<tr>
<td>Binary</td>
<td>Decimal</td>
</tr>
<tr>
<td>0 0 0</td>
<td>1 0 0 0 1 1 1 1</td>
</tr>
<tr>
<td>0 0 1</td>
<td>1 1 1 1 1 1 1 1</td>
</tr>
<tr>
<td>0 1 0</td>
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</tr>
<tr>
<td>1 1 1</td>
<td>1 1 0 0 1 1 0 0</td>
</tr>
</tbody>
</table>

Basic Memory Operations

- Memory operations require the following:
  - **Data** - data sent to, or read from, memory if required by the operation.
  - **An Address** - this is used to specify a range of indices the memory is to operate on. The address lines carry this information to the memory unit. Typically: \( N \) bits specify \( 2^{*N} \) words.
  - **An operation** - Information sent to the memory and interpreted as control information which specifies the type of operation to be performed. Typical operations are READ DATA, and WRITE DATA. Others are READ followed by WRITE and a variety of new operations associated with delivering block of data.
Basic Memory Operations (Continued)

- **Read Memory** -- These operations are used to read a data value stored in memory:
  - Place a valid address on the address lines.
  - Wait for the read data to become stable.
- **Write Memory** -- These operations are used to write a data value to memory:
  - Place a valid address on the address lines and valid data on the data lines.
  - Assert memory write enable line.
- Sometimes the read or write enable line is defined as a clock with precise timing information (e.g. Read Clock, Write Strobe). Sometimes it is just an interface signal. Sometimes memory must acknowledge that it has completed the operation.

Memory Operation Timing

- **The most basic memories are asynchronous**
  - Storage is performed by latches or storage of electrical charge
  - Do not use a clock
- **Controlled by application of control inputs and address**
- **Timing of signal application is critical to the operation**
- **See Figure 6-4 in text**
  - Control Signals:
  - Relative timing of signals for Write and Read
RAM Integrated Circuits

- Types of Random Access Memory (RAM)
  - **Static** – Information stored in latches
  - **Dynamic** – Information stored as electrical charges on capacitors
    - Charge “leaks” off
    - Refresh required

- Dependence on Power Supply
  - Volatile – Lose stored information when power turned off
  - Non-Volatile – Retains information when power turned off

Static RAM Cell

- Array of storage cells used to implement static RAM
- Each storage cell consists of:
  - A latch
  - Cell write logic
  - Cell read logic
- See Figure 6-5 in text for example – A logical representation of electronic circuitry
  - SR Latch for storage
  - Select input for control
  - Dual Rail Data Inputs B and B
  - Dual Rail Data Outputs C and C
Static RAM Bit Slice

- Represents all of the circuitry that is required to store multiple 1-bit words
- See Figure 6-6 in text as an example
  - Multiple RAM cells
  - Control Lines:
    - Word select i – one for each word
    - Read/Write
    - Bit Select
  - Data Lines:
    - Data in
    - Data out

n-Word 1-Bit RAM IC

- To build a RAM IC from a RAM slice, we need:
  - A decoder to decode the log2n address lines to n word select lines
  - A 3-state buffer on the data output to permit RAM ICs to be combined into a RAM with c n words
- See Figure 6-7 in text as an example
  - Add 4-to 16 decoder with address inputs and word select outputs
  - Add 3-state buffer controlled by chip select
3-state Buffers and Logic

- Three-State Logic -- Sometimes called tri-state logic but tri-state is a registered trademark of National Semiconductor -- has three states for logic levels:
  1. Active high state (output is driven high).
  2. Active low state (output is driven low).
  3. High impedance (Hi-Z) state (output is not driven).

- 3-State Logic is especially useful for replacing "open collector" wire-OR or wire-AND oriented busses.
- Often registers made of latches and flip-flops come equipped with three-state outputs.
- Three-state is commonly used for memory components, too

3-State Buffer Basics

- The basic 3-State Buffer is shown:
  - Hi-Z: Means the output is not "driven".
  - The output will "float" to some level which is usually neither "1" nor "0" in this state.
  - When EN = "1", the output will follow the input.
  - Buffer can also invert data
  - EN can be inverted signal

<table>
<thead>
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<th>EN</th>
<th>IN</th>
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<tr>
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3-State Logic Basics

- Making Multiplexers with Tri-state Devices:

<table>
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<th>EN0</th>
<th>IN1</th>
<th>IN0</th>
<th>OL</th>
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<td>0</td>
<td>X</td>
<td>X</td>
<td>Hi-Z</td>
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<td>X</td>
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<td>1</td>
<td>damage</td>
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</table>

Memory arrays can be very large =>

- Large decoders
- Large fanouts for the bit lines

The decoder size and fanouts can be reduced by using a coincident selection in a 2-dimensional array

- Uses 2 decoders one for words and one for bits
- Word select becomes Row select and Bit select becomes Column select

See Figure 6-10 for example

- A_3, A_2 used for Row select and A_1 and A_0 for Column select
RAM ICs with > 1 Bit/Word

- Word length can be quite high.
- To better balance the number of words and word length, use ICs with > 1 bit/word
- See Figure 6-11 for example
  - 2 Data input bits
  - 2 Data output bits
  - Row select selects 4 rows
  - Column select selects 2 pairs of columns