Chapter 4 in *Logic and Computer Design Fundamentals* by Mano and Kime deals with gate delays and flip-flop timing parameters, but does not explicitly relate these to the clock frequency and corresponding speed of operation of the circuit. Here we consider the principal circuit timing parameter, the maximum allowable clock frequency $f_{\text{max}}$. First of all, the clock frequency is just the inverse of the clock period. So, the maximum allowable clock frequency corresponds to the minimum allowable clock period $t_p$. In order to determine how small we can make the clock period, we need to determine the events that take place during that period. These events are shown in Figure 2-1 for edge-triggered and (non-D type) master-slave flip-flops. For the positive edge-triggered flip-flop, when the positive edge of the clock occurs, all of the flip-flops in the circuit could potentially change. We assume that with respect to such changes, we wait for the slowest of all flip-flops to change in its slowest direction of change high(H) to low(L) or low(L) to high(H). This longest propagation delay of any flip-flop in the circuit can be denoted by as $\max (t_{PHL}, t_{PLH})_{FF}$ and is shown in Figure 2-1(a).
After the flip-flops have changed, then the changes must propagate through the combinational logic of the circuit. The longest time that this can take is defined as the maximum combinational delay from flip-flop output to flip-flop input in the circuit which we denote by $\text{max} (t_{\text{COMB}})$ and also show in Figure 2-1(a). We are assuming here that the occurrence of the primary input changes are no later than the change of the slowest flip-flop and that the delays from the primary inputs to the flip-flop inputs are no more than $\text{max} (t_{\text{COMB}})$. This assumption is based on the notion that the primary inputs come directly from storage elements no slower than the slowest flip-flop. If this is not the case, alternative calculations must be used. The calculation of $\text{max} (t_{\text{COMB}})$ can be relatively complicated if MSI circuits or functional blocks are involved. On the other hand, if only gates are involved and there is a fairly uniform worst case value for gate delay, it may simply be the number of gates in the longest path from flip-flop output to flip-flop input times that maximum gate delay.

After the signals have propagated through the combinational logic and reached all of the flip-flop inputs, then a time interval equal to longest setup time of any of the flip-flops must occur before the next positive clock edge. We denote this interval by $\text{max} (t_{\text{su}})$ and show it in Figure 2-1(a) as well.

Note that if we are using a negative edge-triggered flip-flop, the same three time intervals apply relative to the negative edge instead of the positive edge. For (non-D type) master-slave flip-flops, $\text{max} (t_{\text{su}})$ corresponds to the length of time the clock pulse is at the level which enables the inputs as shown in Figure 2-1(b).

We have now determined the events that must occur between consecutive clock edges and assigned times to these events. To obtain the minimum clock period, we simply sum up these times:

$$ t_p = \text{max} (t_{\text{PHL}}, t_{\text{PLH}})_{FF} + \text{max} (t_{\text{COMB}}) + \text{max} (t_{\text{su}}) $$

This calculation can be illustrated by an example. Suppose that the longest flip-flop delay is 2 ns (nanosecond = $10^{-9}$ seconds) giving $\text{max} (t_{\text{PHL}}, t_{\text{PLH}}) = 2$ ns. Suppose that the longest combinational path consists of 15 NAND gates each with a longest delay of 1 ns, giving $\text{max} (t_{\text{COMB}}) = 15$ ns. Finally, suppose that the longest setup time among the flip-flops, $\text{max} (t_{\text{su}})$, is 1.5 ns. From this data, we obtain a value for the minimum clock period of $2 + 15 + 1.5 = 18.5$ ns. This gives a maximum clock frequency of 54.05 MHz ($\text{megahertz} = 10^6$ cycles per second). We note that if $t_p$ is too large to meet the circuit specifications, we must either employ faster components or must change the circuit design to reduce the various delays through the circuit while still performing the desired function.

It is interesting to note that the hold time $t_h$ does not appear in the clock period equation. It relates to another timing constraint equation dealing with one or both of two specific situations. In one case, output changes arrive at the inputs of one or more flip-flops too soon. In the other case, the clock signals reaching one or more flip-flops are somehow delayed, a condition referred to as clock skew. Clock skew also can affect the maximum clock frequency.