1. (bitwise logic) Problem 7-4, text book, p. 356
   Answer:
   \[
   \begin{array}{c}
   1001 \ 1001 \\
   1100 \ 0011 \\
   1000 \ 0001 \quad \text{AND} \\
   1101 \ 1011 \quad \text{OR} \\
   0101 \ 1010 \quad \text{XOR}
   \end{array}
   \]

2. (bitwise logic) Problem 7-5, text book, p. 357
   Answer:
   (a) AND, 1010 1010 1010 1010  
   (b) OR, 1111 0000 0000 0000  
   (c) XOR, 0000 1111 1111 0000

3. (registers) Problem 7-7, text book, p. 357
   Answer:
   Connections to MUX data input 0 and data input 3 remain the same. $Q_{i-1}$ is connected to MUX data input 2 instead of MUX data input 1. Finally, $Q_0$ is connected to MUX data input 1.

4. (ripple counter) Problem 7-10, text book, p. 357
   Answer:
   a) 5 
   b) 8

5. (synchronous counter) Problem 7-12, text book, p. 357
   Answer:
   ![Diagram](image1)

6. (synchronous counter) Problem 7-14, text book, p. 358 (use Figure7-14)
   Answer:
   ![Diagram](image2)
7. (synchronous counter) Problem 7-18, text book, p. 358
   Answer:
   \[
   \begin{array}{c|c|c|c|c|c|c}
   \text{Present state} & A & B & C & \text{Next state} & A & B & C \\
   \hline
   0 & 0 & 0 & 0 & 0 & 0 & 1 \\
   0 & 0 & 1 & 0 & 1 & 1 & 0 \\
   0 & 1 & 0 & 1 & 1 & 0 & 0 \\
   0 & 1 & 1 & 1 & 0 & 1 & 0 \\
   1 & 0 & 0 & 1 & 1 & 0 & 0 \\
   1 & 1 & 0 & 0 & 0 & 0 & 0 \\
   \end{array}
   \]
   \[D_A = \overline{ABC} + \overline{AB} \]
   \[D_B = C + \overline{A}B \]
   \[D_C = \overline{A}B \]

8. (register transfer) Problem 7-21, text book, p. 358
   Answer:
   ![Register Transfer Diagram]

9. (register transfer) Problem 7-25, text book, p. 359
   Answer:
   ![Register Transfer Diagram]
   This is the suggested solution from Mano & Kime.
   There is a way to optimize this solution even more.

10. (register transfer) Problem 7-27, text book, p. 360
    Answer:
    ![Register Transfer Diagram]
11. (register transfer) Problem 7-31, text book, p. 360

**Answer:**

```
a) Destination <- Source Registers
R0 <- R1, R2
R1 <- R4
R2 <- R3, R4
R3 <- R1
R4 <- R0, R2

b) Source Registers -> Destination
R0 -> R4
R1 -> R0, R3
R2 -> R0, R4
R3 -> R2
R4 -> R1, R2

c) The minimum number of buses needed for operation of the transfers is three since transfer Cb requires three different sources.
```

12. (register transfer) Problem 7-33, text book, p. 361

**Answer:**

```
Two clock cycles minimum
```


**Answer:**

```
<table>
<thead>
<tr>
<th>Shifts</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0111</td>
<td>0011</td>
<td>0001</td>
<td>1000</td>
<td>1100</td>
</tr>
<tr>
<td>B</td>
<td>0101</td>
<td>0010</td>
<td>0001</td>
<td>0000</td>
<td>0000</td>
</tr>
<tr>
<td>C</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
```