1. (RAM) Problem 9-1, text book, p. 427
   Answer:
   a) $A = 14, D = 8$    b) $A = 18, D = 16$    c) $A = 26, D = 32$    d) $A = 31, D = 8$

2. (RAM) Problem 9-2, text book, p. 427
   Answer:
   a) $2^{14}$    b) $2^{10}$    c) $2^{28}$    d) $2^{31}$

3. (RAM) Problem 9-4, text book, p. 428
   Answer:
   Number of bits in array = $2^{16} \cdot 2^4 = 2^{20} = 2^{10} \cdot 2^{10}$
   Row Decoder size = $2^{10}$
   a) Row Decoder = 10 to 1024, AND gates = $2^{10} = 1024$
      Column Decoder = 6 to 64, AND gates = $2^6 = 64$
      Total AND gates required = 1024 + 64 = 1088
   b) $(32000)_{10} = (01111110100 \ 0000000)_{2}$, Row = 500, Column = 0

4. (DRAM) Problem 9-6, text book, p. 428
   Answer:
   14 row pins + 13 column pins = $2^{27} = 128M$ addresses

5. (DRAM) Problem 9-7, text book, p. 428
   Answer:
   With 4-bit data, the RAM cell array contains $64M = 2^{26}$ words.
   The number of address pins is $26/2 = 13$.

6. (status bits) Problem 10-2, text book, p. 476
   Answer:
   \[
   \begin{align*}
   C &= C_4 \\
   V &= C_3 \oplus C_7 \\
   Z &= \overline{F_7 + F_6 + F_5 + F_4 + F_3 + F_2 + F_1 + F_0} \\
   N &= F_7
   \end{align*}
   \]
7. (ALU) Problem 10-5, text book, p. 477

Answer:

[Diagram of ALU with connect to Cin for first stage.]

This is the suggested solution from Mano & Kime.
There is a way to optimize this solution even more.

8. (barrel shifter) Problem 10-8, text book, p. 477

Answer:

(a) 0101  (b) 0110  (c) 0101  (d) 0110

9. (control word) Problem 10-9, text book, p. 477

Answer:

<table>
<thead>
<tr>
<th>DA</th>
<th>AA</th>
<th>BA</th>
<th>MB</th>
<th>FS</th>
<th>MD</th>
<th>RW</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) 000</td>
<td>001</td>
<td>111</td>
<td>0010</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>(b) 111</td>
<td>000</td>
<td>000</td>
<td>0110</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>(c) 111</td>
<td>111</td>
<td>110</td>
<td>0110</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>(d) 011</td>
<td>100</td>
<td>0110</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(e) 000</td>
<td>111</td>
<td>111</td>
<td>0001</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>(f) 010</td>
<td>100</td>
<td>1</td>
<td>0101</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>(g) 000</td>
<td>010</td>
<td>011</td>
<td>0101</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>(h) 110</td>
<td>101</td>
<td>1</td>
<td>11011000</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

This is the suggested solution from Mano & Kime.
There is a way to optimize this solution even more.


Answer:

\[
\begin{align*}
R3 &\leftarrow R3 + R1 \leftarrow 01100111 \\
R4 &\leftarrow R4 \land R1 \leftarrow 01110100 \\
R5 &\leftarrow R5 \land R1 \leftarrow 01101100 \\
R1 &\leftarrow R1 \leftarrow 11011111
\end{align*}
\]

R1 ... R7 = i, D, g, t, l, a, i Unscrambled is Digital

11. (pipelining) Problem 10-12, text book, p. 478

Answer:

(a) \( f = 1/14ns \approx 71.4 \text{ MHz} \)
(b) Stage 1: AC, Delay = 6ns, \( f = 1/6ns = 166.7 \text{ MHz} \)
(c) Stage 1: AB, Delay = 3ns,
Stage 4: E, Delay = 4ns, \( f = 1/4ns = 250 \text{ MHz} \)

Stage 2: D, Delay = 4ns,
Stage 3: C, Delay = 3ns,
Stage 3: D, Delay = 4 ns,
12. (single-cycle computer) Problem 10-16, text book, p. 479
Answer:

<table>
<thead>
<tr>
<th>Instruction/Register Transfer</th>
<th>DA</th>
<th>AA</th>
<th>BA</th>
<th>MB</th>
<th>FS</th>
<th>MD</th>
<th>RW</th>
<th>MW</th>
<th>PL</th>
<th>JB</th>
</tr>
</thead>
<tbody>
<tr>
<td>R[0] ← R[7] + R[3]</td>
<td>100</td>
<td>111</td>
<td>011</td>
<td>0</td>
<td>1010</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>x</td>
</tr>
<tr>
<td>R[1] ← M[R[4]]</td>
<td>001</td>
<td>100</td>
<td>xxx</td>
<td>x</td>
<td>xxxx</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>x</td>
</tr>
<tr>
<td>R[2] ← R[5] + 2</td>
<td>010</td>
<td>101</td>
<td>xxx</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>x</td>
</tr>
<tr>
<td>R[3] ← 51R[6]</td>
<td>011</td>
<td>xxx</td>
<td>110</td>
<td>0</td>
<td>1110</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>x</td>
</tr>
<tr>
<td>IF R[4] = 0 then PC ← PC + 8PC</td>
<td>xxx</td>
<td>100</td>
<td>xxx</td>
<td>x</td>
<td>www</td>
<td>x</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Answer:

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Code</th>
<th>Registers/Memory changed</th>
</tr>
</thead>
<tbody>
<tr>
<td>SUB R0, R1, R2</td>
<td>000 101 000 001 010</td>
<td>R0 = -1</td>
</tr>
<tr>
<td>SUB R3, R4, R5</td>
<td>000 001 011 100 101</td>
<td>R3 = -1</td>
</tr>
<tr>
<td>SUB R6, R7, R0</td>
<td>000 0101 110 111 000</td>
<td>R6 = 6</td>
</tr>
<tr>
<td>SUB R0, R0, R3</td>
<td>000 0101 000 000 011</td>
<td>R0 = 0</td>
</tr>
<tr>
<td>SUB R0, R0, R6</td>
<td>000 0101 000 000 110</td>
<td>R0 = 0</td>
</tr>
<tr>
<td>ST R7, R0</td>
<td>010 0000 000 111 000</td>
<td>R0 = -6</td>
</tr>
<tr>
<td>LD R7, R6</td>
<td>011 0000 111 110 000</td>
<td>M[7] = -6</td>
</tr>
<tr>
<td>ADD R0, R6, 6</td>
<td>100 010 000 110 000</td>
<td>R0 = 6</td>
</tr>
<tr>
<td>ADD R3, R6, 3</td>
<td>100 0101 110 011</td>
<td>R3 = 9</td>
</tr>
</tbody>
</table>

Answer:


Both V and C are 0