Homework #5 (Spring 1999)

Homework 3 covers materials in chapters 7 and 8
Problems labeled with an (*) are challenging problems
You need NOT turn in the homework. However, you are strongly advised to work it out. Short solutions will be posted on course web home page shortly. We encourage you to work with your classmates as a group so that you can learn from each other.

17. Problem 8-10 text book, page 420.

26. (Bus Transfer) The following register transfer operations are to be implemented on two different register transfer bus structures shown below.

K1: \[ R1 \leftarrow R2 \]
K2: \[ R3 \leftarrow R2 \]
K3: \[ R3 \leftarrow R0 \]
K4: \[ R2 \leftarrow R1 \]
A. Single Bus Structure

B. Multiple Bus Structure

(a) In the table below, write a sequence of register transfer operations for each bus structure. Use one line per clock cycle, and separate micro-operations that may proceed in parallel using a comma. You should use minimum number of clock cycles required to realize all four micro-operations for each bus structure.

<table>
<thead>
<tr>
<th>A. Single Bus Operation Sequence</th>
<th>B. Multiple Bus Operation Sequence</th>
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<tbody>
<tr>
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</tbody>
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(b) Given the multiple bus transfer structure B, and given that $SA_1 = K1 + K2$, and $SA_0 = 0$. Write expression for $SB_1$, and $SB_0$ below.

<table>
<thead>
<tr>
<th>control</th>
<th>Boolean Function</th>
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</thead>
<tbody>
<tr>
<td>$SB_1 =$</td>
<td></td>
</tr>
<tr>
<td>$SB_0 =$</td>
<td></td>
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</tbody>
</table>