

**Department of Electrical and Computer Engineering  
University of Wisconsin–Madison**

**ECE 553:** Testing and Testable Design of Digital Systems  
Fall 2010-2011

**Final Examination**

**CLOSED BOOK**

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Date: December 21, 2010  
Place: Room 1153 Mechanical Engineering  
Time: 5:05 - 7:05 PM  
Duration: 120 minutes

PROBLEM	TOPIC	POINTS	SCORE
1	Test Economics	12	
2	Testability Analysis	13	
3	Test Generation	13	
4	Memory Test	11	
5	Pseudo-exhaustive test	10	
6	DFT: Full and Partial scan	11	
7	Partial scan	9	
8	Boundary Scan	9	
9	BIST	12	
TOTAL		100	

Last Name: \_\_\_\_\_

First Name: \_\_\_\_\_

Show your work carefully for both full and partial credit.

You will be given credit only for what appears on your exam. **Use extra sheets if you need more space to write**

## 1. (12 points) Test Economics

A manufacturer of ICs uses the following yield equation for its product.

$$Y(T) = [1 + Taf/\beta]^{-\beta}$$

In this equation  $T$  is fault coverage,  $a$  is area of the chip, and  $f$  and  $\beta$  are process parameters. The values of the process parameters are as follows:

$f = 1.48$  faults/ sq. cm. and  $\beta = 0.14$

- (a) (6 points) For the area of chip to be 0.95 sq cm and fault coverage to be 94% determine the percent yield and defect level in parts per million (PPM) for this product.

- (b) (6 points) The manufacturer is not too satisfied with this yield and defect level. It wishes to reduce the defect level to below 1000 PPM but realizes that such a drastic change in defect level will require DFT that will increase the chip area by 10%. The manufacturer will continue to use the the same process for its modified product.

- i. (2 points) What will be the yield of the modified product if the manufacturer does not change the tests and test strategy?

- ii. (4 points) Determine the fault coverage the manufacturer will need to meet its goal of reduced defect level.

2. (13 points) Testability Analysis

For a part of a large combinational circuit shown in Figure 1, compute the SCOAP controllability and observability values for each line listed in the table below. Some of the values are provided and they are sufficient to deduce all the remaining values. Some of the values may in the table for your consistency check.

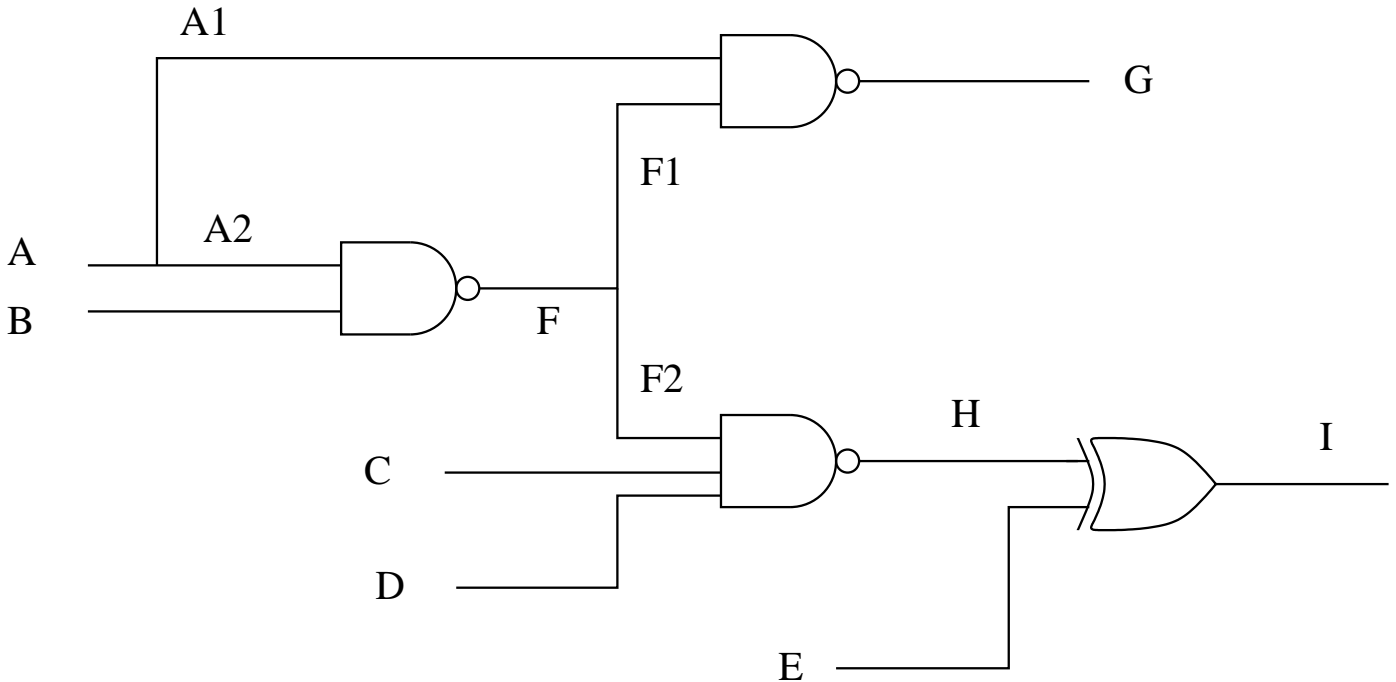


Figure 1: Testability analysis values

Line #	CC0	CC1	CO	Line #	CC0	CC1	CO
A		30		A2		30	
B				F	70		74
C	25	30		F1	70		
D	50	20		F2	70		
E	12	35	37	G	51	46	50
				H			
A1		30		I			

3. (13 points) Test Generation

Consider the combinational circuit given below. A PODEM like test generator creates a decision tree shown below during the test generation process for the fault marked (line L stuck-at 0) in the circuit.

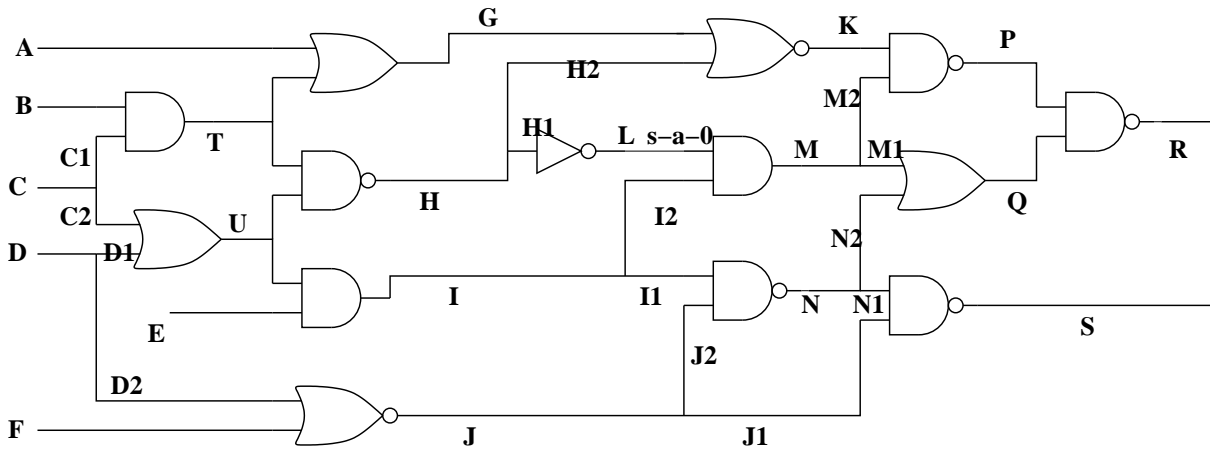


Figure 2: Combinational Circuit Test Generation

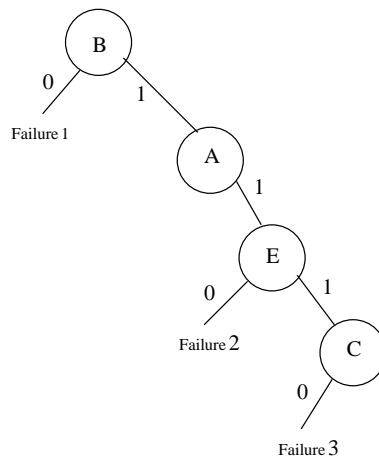


Figure 3: Decision Tree for Combinational Circuit Test Generation

- (a) (6 points) For each decision shown in the decision tree complete all the implications in the following table. You need not specify the line values that are not labeled in the figure.



4. (11 points) Memory testing

A 256MB RAM has 28 address inputs and 8 data I/O lines. Internally the memory also contains an *even parity* bit for each byte. The parity is generated and checked internally for potential errors. Each byte and the corresponding parity bit are arranged in the memory array as shown below in (a). In this arrangement  $d0 \dots d7$  are the data bits of a 8-bit data byte and the  $P$  is the even parity bit corresponding to the data byte. Note that bit  $P$ , placed between  $d3$  and  $d4$ , is internally generated based on the data values in the byte.



(a) Organization of a Byte and the Parity bit

To test this RAM 8-bit bytes are written and read directly. Eight test patterns,  $B(0), \dots, B(3), \overline{B(0)}, \dots, \overline{B(3)}$ , used to test the RAM are shown in (b) below:

Name	8-bit Pattern							
	d0	d1	d2	d3	d4	d5	d6	d7
$B(0)$	0	0	0	0	0	0	0	0
$B(1)$	0	1	0	1	0	1	0	1
$B(2)$	0	0	1	1	0	0	1	1
$B(3)$	0	0	0	0	1	1	1	1
$\overline{B(0)}$	0	1	1	1	1	1	1	1
$\overline{B(1)}$	1	0	1	0	1	0	1	0
$\overline{B(2)}$	1	1	0	0	1	1	0	0
$\overline{B(3)}$	1	1	1	1	0	0	0	0

(b) Eight Test Patterns to Test RAM

The test algorithm used to test the RAM is given below:

```

For i := 0 to 3 do
** Initialization step ***
    For address := 0 to 256M-1 do
        begin write  $B(i)$  end;

** Test steps ***
    begin
        for address := 0 to 256M-1 do
            begin
                Read  $B(i)$ 
                Write  $\overline{B(i)}$ 
                Read  $\overline{B(i)}$ 
            end;
        end;
    end;

```

Answer the following questions:

- (a) (**1 points**) What will be the contents of each cell in the RAM after the initialization step of the algorithm is complete for  $i = 0$ ?
  
- (b) (**2 points**) At the end of the execution of the test step for  $i = 2$  what will be the contents of each byte and the corresponding parity bit in the RAM?
  
- (c) (**4 points**) Let us consider three bits  $d3$ ,  $P$  and  $d4$  in RAM. At the end of complete testing how many and what distinct three bit patterns would have been applied to these three bits in RAM?
  
- (d) (**4 points**) Let us consider three consecutive addresses in RAM, and the bits  $d2$  of these addresses. At the end of complete testing how many and what distinct three bit patterns would have been applied to these three bits in RAM?





6. (11 points) **DFT: Full and Partial Scan**

Block diagram level description of an embedded circuit is shown in Figure 5. This circuit has a total of 105 flip-flops that are grouped into three blocks containing different number of flip-flops shown in the figure. The primary inputs and primary output of combinational logic block are also shown in the figure.

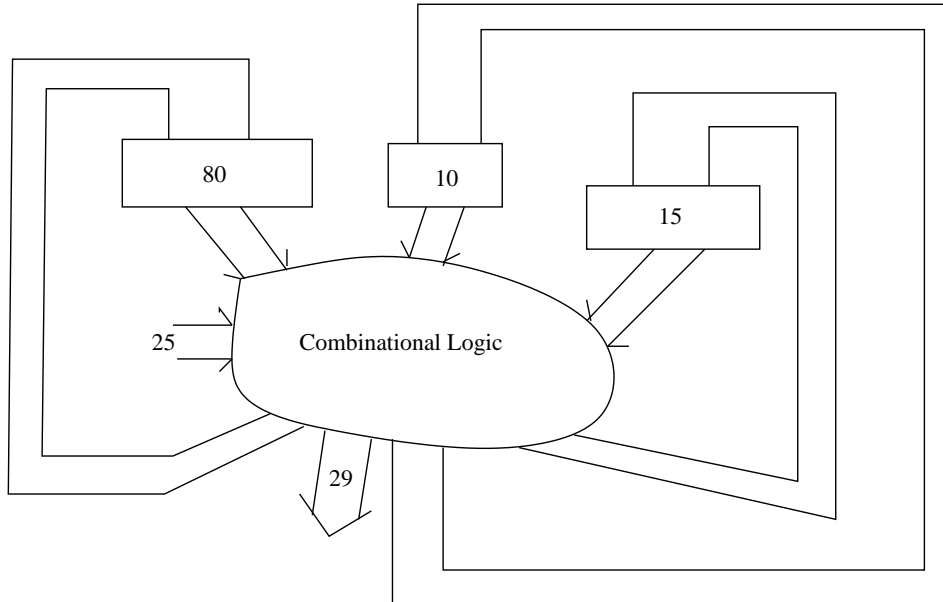


Figure 5: Circuit with Full and Partial Scan.

- (a) (4 points) Assume that this circuit uses full scan DFT method. Now answer the following:
- i. (1 point) What will be the total number of inputs and total number of outputs of this circuit for the purpose of test generation.
  - ii. (1 point) How many scan clocks will it take to scan-in one test vector for testing the combinational logic block.
  - iii. (2 points) If the number of tests required to reach 100% fault coverage of the combinational logic is 752, determine the the total number of clocks (scan clocks and system clocks) required to apply all tests using scan testing. You can assume that the scan chain is fault free and does not need to be tested.

- (b) (**5 points**) Assume that the circuit uses partial scan DFT method. The two groups of FFs consisting of 10 and 15 FFs are made scanable. Further, these two groups form two parallel scan chains. Now answer the following:
- i. (**1 point**) What will be the total number of inputs and outputs of this circuit for the purposes of test generation. Note in this case the test generator will be a sequential test generator
  
  - ii. (**1 points**) How many scan clocks will it take to scan-in each pattern during testing using partial scan with two scan chains.
  
  - iii. (**3 points**) Assume that the number of test vectors generated by a sequential test generator to test the circuit with partial scan for 98% fault coverage is 2540. Determine the the total number of clocks (scan clocks and system clocks) required to apply all tests using partial scan testing. You can assume that the scan chain is fault free and does not need to be tested. You must include a brief explanation for your answer.
- (c) (**2 points**) If the above circuit has both partial and full scan capabilities, suggest a testing strategy that will not require as many clock cycles to test the circuit as full-scan while offering a 100% fault coverage.

## 7. (9 points) Partial Scan

S-graph of a sequential circuit consisting of 10 FFs is shown in Figure 6. Answer the following:

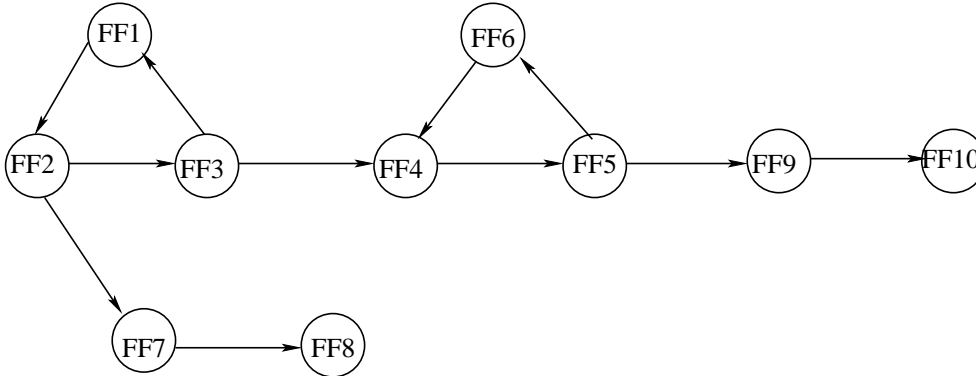


Figure 6: S-graph of a Sequential Circuit.

- (a) (1 point) How many cycles this circuit has?
- (b) (1 point) What is the smallest number of FFs that should be included in the scan path to break all cycles.
- (c) (3 points) Find a smallest set of FFs for inclusion in the scan path that will break all cycles while **minimizing** the sequential depth of the circuit. List the FFs to be included in the scan path and the depth of the circuit.
- (d) (4 points) Find a smallest set of FFs for inclusion in the scan path that will break all cycles while **maximizing** the sequential depth of the circuit. List the FFs to be included in the scan path and identify the longest path in the circuit.

**8. (9 points) Boundary scan and general problems**

A board contains five ICs all of which have boundary scan. The information relevant to this problem about these ICs is given in the table below:

Device information	IC-1	IC-2	IC-3	IC-4	IC-5
Number of input pins	121	150	98	75	50
Number of output pins	51	75	129	175	250
Number of bidirectional pins	11	15	0	15	0
Number of three state pins	5	5	0	17	20
Bits in Instruction reg	4	3	5	3	7
Bits in Device ID reg	45	45	52	50	45

Answer the following:

- (a) **(1 points)** What is the length of Boundary scan data register (number of flip-flops in the boundary scan) for the IC-3?
  
- (b) **(1 points)** What is the length of Boundary scan data register (number of flip-flops in the boundary scan) for the IC-5?
  
- (c) **(1 points)** What is the length of Boundary scan data register (number of flip-flops in the boundary scan) for the IC-1?
  
- (d) **(1 points)** All five ICs form a single boundary scan chain on the board. How many extra pins the board will have to make use of the boundary scan feature of the ICs.
  
- (e) **(2 points)** Assuming that the TAP controller on each ICs is in Shift-IR state, how many test clocks (TCK) are required to load the instruction registers of all ICs?
  
- (f) **(2 points)** Assume that IC-1, IC-2, IC-4 and IC-5 are in bypass modes and the TAP controller on each ICs is in Shift-DR state, how many test clocks (TCK) are required to load the boundary register of IC-3? You can assume that the ICs are connected in sequential order.
  
- (g) **(1 points)** Are the power and ground pins placed in the boundary scan data register?

## 9. (12 points) BIST

Answer the following and you must show your work for full credit.

- (a) (4 points) Realization of a 6-bit mixed mode (internal/external EOR) Linear Feedback Shift Register (LFSR) is given in the Figure 7 below along with the notation used to label the flip-flops.

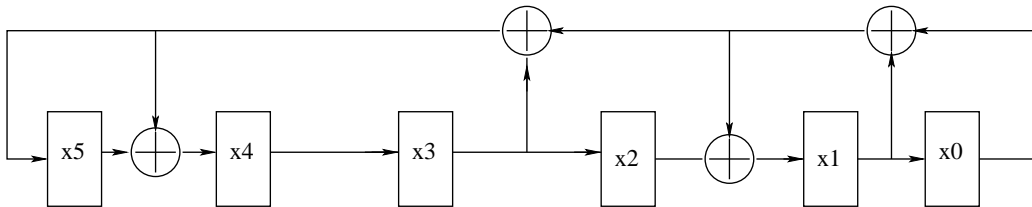


Figure 7: A mixed mode linear feedback shift register

Write the companion matrix  $T_s$  for the above LFSR by completing the following matrix equation.

$$\begin{bmatrix} x0(t+1) \\ x1(t+1) \\ x2(t+1) \\ x3(t+1) \\ x4(t+1) \\ x5(t+1) \end{bmatrix} = \begin{bmatrix} & & & & & \\ & & & & & \\ & & & & & \\ & & & & & \\ & & & & & \\ & & & & & \end{bmatrix} \begin{bmatrix} x0(t) \\ x1(t) \\ x2(t) \\ x3(t) \\ x4(t) \\ x5(t) \end{bmatrix}$$

- (b) (2 points) Give an internal-EOR (modular) realization of the following polynomial. Label the variables correctly.

$$x^5 + x^4 + x^2 + 1$$

- (c) (**2 points**) Give an external-EOR (standard) realization of the following polynomial. Again label the variables correctly.

$$x^5 + x^4 + x^2 + 1$$

- (d) (**2 points**) The polynomial  $x^5 + x^4 + x^2 + 1$  is not irreducible. Find one of its divisors and write the quotient.

- (e) (**2 points**) Consider the standard LFSR shown in Figure 8 below. Find its non trivial initial state that will cause the LFSR to cycle after visiting 5 distinct states. Show all the states that will result when this LFSR is used with the initial state found by you.

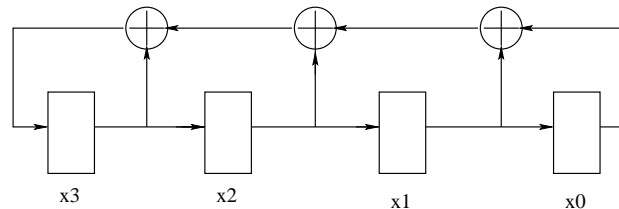


Figure 8: A standard linear feedback shift register