Department of Electrical and Computer Engineering
University of Wisconsin–Madison

ECE 553: Testing and Testable Design of Digital Systems
Fall 2011-2012

Final Examination

SOLUTION

CLOSED BOOK

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Date: December 17, 2011
Place: Room 2540 Engineering Hall
Time: 2:45 - 4:45 PM
Duration: 120 minutes

PROBLEM	TOPIC	POINTS	SCORE
1	Test Economics	15	
2	Fault Simulation	10	
3	Test Generation	6	
4	Test Compaction	8	
5	Memory Test	14	
6	Pseudo-exhaustive test	10	
7	DFT: Full and Partial scan	16	
8	BIST	12	
9	Boundary Scan	9	
TOTAL		100	

Last Name: SOLUTION

First Name: ______________________________

Show your work carefully for both full and partial credit.
You will be given credit only for what appears on your exam. **Use extra sheets if you need more space to write**

1. (**15 points**) **Test Economics**

   A board manufacturer uses 25 ICs of the same kind. The IC vendor provided the following specifications of its product:

   Area of the IC, A = 0.75 sq cm.
   Fault density, f = 1.45 faults/sq cm
   Clustering factor, $\beta = 0.11$
   Fault coverage, T = 90%
   Cost of the IC = \$ 4.00

   Now answer the following, and while answering you must show your work.

   (a) (**3 points**) Determine the Defect Level of the product sold by the IC vendor.

   Using the equation for Defect level $DL = 1 - \left(\frac{\beta+TAf}{\beta+Af}\right)^{\beta}$ and substituting T = 0.90, A = 0.75, f = 1.45 and $\beta = 0.11$
   we get $DL(T) = 0.0104179$, i.e. 10418 ppm

   (b) (**5 points**) Determine the average cost of producing a good board. You can ignore the cost of printed circuit, the board hardware, and the test equipment.

   Probability of a board being good is $(1 \ - \ DL)^{25}$. Which is 0.769. Hence the average cost of a good board will be $\frac{25\times4}{0.769}$. which is \$ 129.93.

   (c) (**7 points**) The board manufacturer is willing to pay \$0.50 more for each IC, provided the IC vendor will raise the fault coverage to 95%. Is this a good deal for the board manufacturer? You must provide a quantitative reasoning and you must show your work.

   We can determine the defect level (DL) for T = 0.95. Which is 5100 ppm. Again the probability of a board being good will be 0.880032. This will result into average cost of a board to be $\frac{25\times4.5}{0.88}$. Which is \$127.84.
   Hence, this is a better deal for the board manufacturer.

2. (**10 points**) **Parallel Fault Simulation**

The circuit of Fig 1 is to be simulated using parallel fault simulation method for the following input pattern:

```
A B C   = 1 0 1
```

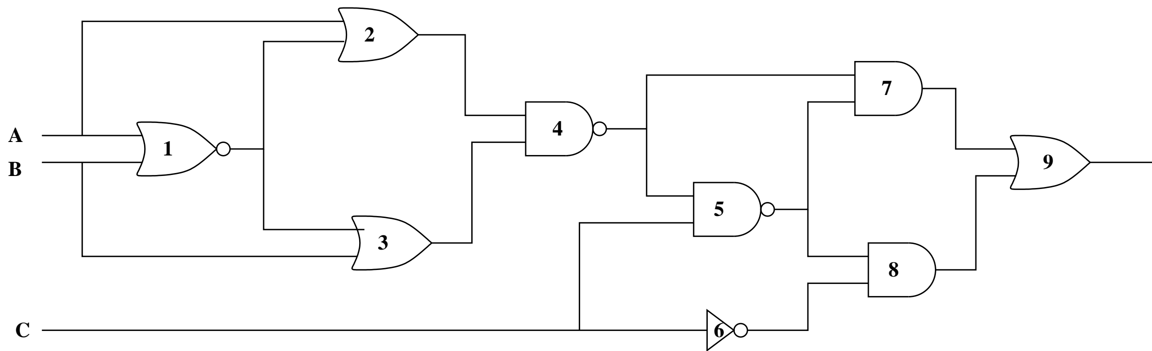

Figure 1: Combinational Circuit for Parallel Fault Simulation

Assuming that the word size of a computer is 5 bits and the bits are numbered from 0 to 4 starting from the right most bit as shown in the Fig 2.

bit 4				bit 0
7/5/1	6/1	4/1	3/1/1	Fault Free

Figure 2: Bits and Faults to be Injected

You are to inject the faults shown in Fig 1 at the bit positions shown in Fig 2. Please pay attention to the correct bit position for each fault. If your choice of positions is different, you will not be given any credit.

(a) (**2 point**) Based on the information provided, marked the lines in the figure, for which the faults are to be simulated.

Faults are marked in the figure 3.

(b) (**8 points**) Enter all the signal line values in the table below as 5 bit values. I have already placed some of the signal values in the table to get you started.

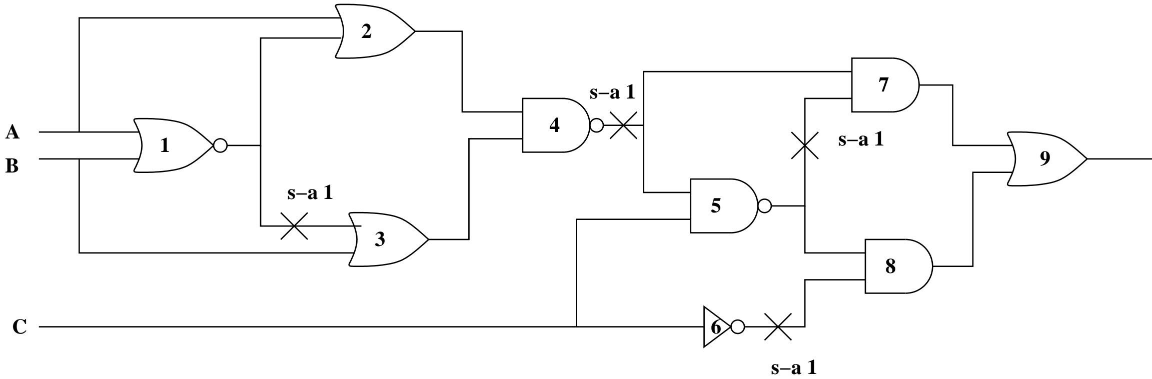

Figure 3: Combinational Circuit for Parallel Fault Simulation Solution

Line Name	Simulated value	Line Name	Simulated value
A	1 1 1 1 1	5/4	1 1 1 0 1
B	0 0 0 0 0	5/C	1 1 1 1 1
C	1 1 1 1 1	5	0 0 0 1 0
1/A	1 1 1 1 1	7/4	1 1 1 0 1
1/B	0 0 0 0 0	7/5	1 0 0 1 0
1	0 0 0 0 0	7	1 0 0 0 0
2/A	1 1 1 1 1	6/C	1 1 1 1 1
2/1	0 0 0 0 0	6	0 1 0 0 0
3/1	0 0 0 1 0	8/5	0 o 0 1 0
3/B	0 0 0 0 0	8	0 0 0 0 0
2	1 1 1 1 1	9	1 0 0 0 0
3	0 0 0 1 0		
4	1 1 1 0 1		

3. (**6 points**) **Test Generation**

A PODEM like test generator is used to generate a test for the fault in a circuit with 8 inputs, A, B, C, D, E, F, G, H. Part of the test generation process which assigns PIs, determines if a backtrack should occur, and the value assigned to each PI is shown in the table below.

Step No.	Objective		PI	*D* front	comment
1	x13 to 0		C=0	-	fault not yet excited
2			B=1	y4	fault excited
3	x12 to 0		A=0	null	backtrack and reverse decision
4			A=1	y5, y6	
5	x16 to 1		E=1	y5, y6	Objective not yet satisfied
6	x16 to 1		G=0	y5	Objective not yet satisfied
7	x16 to 1		F=1	Null	Backtrack and reverse the decision
8			F=0	Null	Backtrack and reverse the decision G=0, Set F=X
9			G=1	y9, y10	
10	x10 to 1		F=0	y11	
11	x19 to 1		H=1	Null	Backtrack and reverse the decision
12			H=0		Success - Test found

(a) (**4 points**) Construct the decision tree for the complete test generation process for arriving at the final test.

See the decision tree in Figure 4

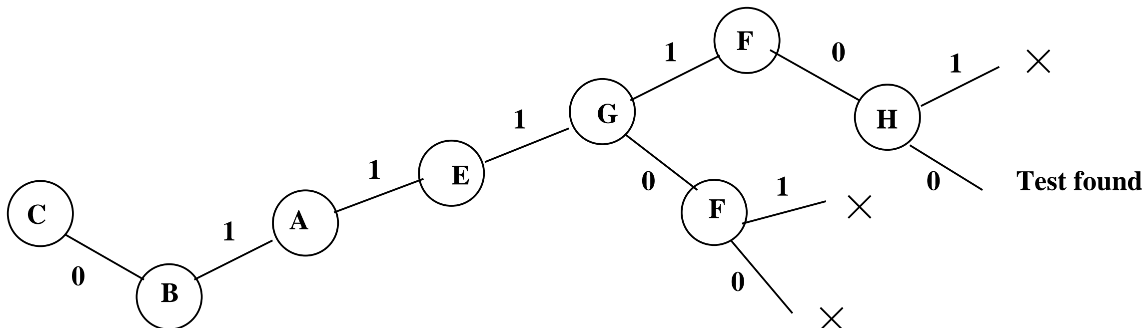

Figure 4: Decision Tree for the test generator

(b) (**2 points**) Write the generated test.

A B C D E F G H = 1 1 0 X 1 0 1 0

4. (**8 points**) **Test Compaction**

   In a test generation process for a combinational circuit six tests, $t_1, t_2, t_3, t_4, t_5, t_6$ are generated to cover a set of given faults. Later it is discovered that we are interested only in a subset of the faults and the subset consists of eight faults, $f_1, f_2, f_3, f_4, f_5, f_6, f_7, f_8$.

   Though simulating the six tests for each of the faults (without fault dropping) we find the detection capability of each test as given below.
   The test t_1 can detect faults f_3 and f_5
   The test t_2 can detect faults f_2 and f_7
   The test t_3 can detect faults f_2, f_3, and f_7
   The test t_4 can detect faults f_1, f_2, and f_7
   The test t_5 can detect faults f_4, and f_6
   The test t_6 can detect faults f_1, f_4, f_6 and f_8

   (a) (**4 points**) If a reverse order fault simulation method is used to reduce the test set what will be test set produced by such a method to detect all the eight faults. Assume that the original test set order is t_1 t_2 ... t_6. Show your work but be brief.

   t_6 detects faults f_1, f_4, f_6 and f_8. Next simulated test t_5 will not detect any new fault. t_4 will detect new faults f_2, and f_7. t_3 will detect new fault f_3. t_2 will not detect any new fault. Lastly, t_1 will detect new fault t_5. Hence the test set so obtained will contain 4 tests, namely t_6, t_4, t_3, and t_1.

   (b) (**4 points**) Find a smallest set of tests that can detect all eight faults. You must show your work other to prove that the set obtained by you is the smallest set.

   We can use cover table appraoch or prove it as follows.

   Fault f_5 is detected by test t_1 alone and similarly the fault f_8 is detected by t_6 alone. Therefore these two tests must be included any test set that detects all faults. The remaining two faults, f_2 and f_7 can be detected by any of the following three tests, t_2 or t_3 or t_4. Hence the smallest test set will contain only three tests.

5. (**14 points**) **Memory testing**

   Answer the following questions related to Memory testing.

   (a) (**4 points**) Consider a memory fault in which a memory cell i changes state from 0 to 1 whenever this cell is read and the content of cell $i+1$ is also 0, but after correctly reading the contents of the cell in question. Write a "March test" for detecting such a fault in a memory array. Use as few march elements as possible and the test length should be as small as possible.

   The following march test has only one march element and it will detect this fault.

$$\{\Downarrow (W0, R0, R0)\}$$

   (b) (**10 points**) Consider the following March algorithm:

$$\{\Uparrow (W0); \quad \Uparrow (R0, W1); \quad \Downarrow (R1)\}$$

   This algorithm is called MARCH-fa-553-2011. You can refer to the three march elements in this algorithm as M1, M2 and M3. This test is applied to a 1M memory array consisting of 1024×1024 bits.

   - (**1 point**) What is the length of this algorithm?

     Test length is 4M

   - (**1 point**) Will this algorithm detect cell all stuck-at faults in the memory array?

     It will detect any stuck-at fault. A s-a 1 fault will be excited in M1 and detected in M2. A s-a 0 fault will be excited in M2 and detected in M3.

   - (**2 points**) Consider a fault in which a writing a 1 to the memory location 1523 causes the cell 249 to change from 1 to 0. Will this test detect such a fault? If yes, when will the fault be excited and when will it be detected. If no, explain.

     This fault will be excited in M2 and detected in M3.

   - (**2 points**) Consider a fault in which a writing a 0 to the memory location 1523 causes the cell 249 to change from 1 to 0, will this test detect such a fault? If yes, when will the fault be excited and when will it be detected. If no, explain.

     This fault is never excited and hence never detected.

   - (**2 points**) Consider a fault in which a writing a 1 to the memory location 4007 causes the cell 429 to change from 0 to 1, will this test detect such a fault? If yes, when will the fault be excited and when will it be detected. If no, explain.

     This fault is also never excited and hence not detected.

- (**2 points**) Consider a fault in which a writing a 0 to the memory location 4007 causes the 429 to change from 0 to 1, will this test detect such a fault? If yes, when will the fault be excited and when will it be detected. If no, explain.

  This fault will be excited in M1 and detected in M2.

6. (**10 points**) **Pseudo-exhaustive testing**

Consider the circuit below in Figure 5. This circuit is to be tested using pseudoexhaustive testing with sensitized partitioning. The partitions are shown in the figure. Note that each gate forms a partition and it must be tested exhaustively using all 4 tests. Also remember when a partition is tested its output must be sensitized to the primary output. Derive

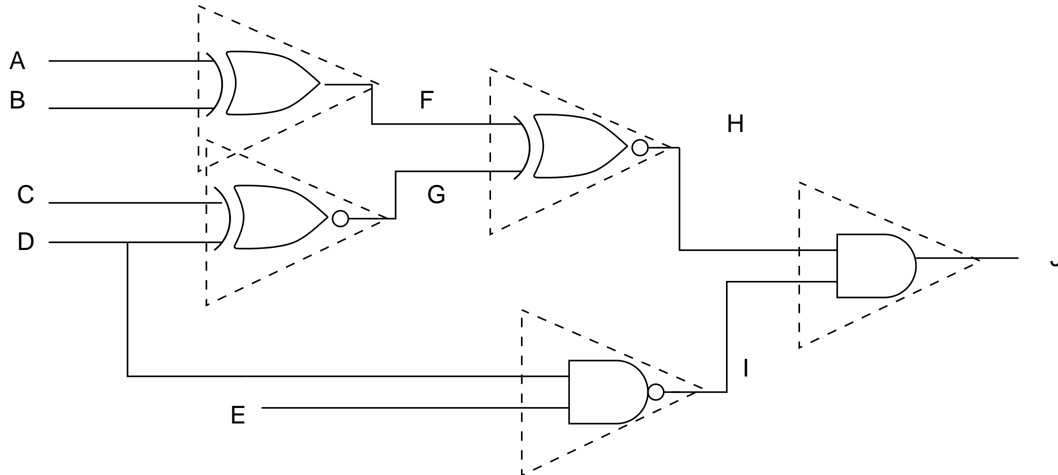

Figure 5: Figure for Pseudoexhaustive Test Generation

a smallest test set (using fewest test vectors) to test this circuit so that each partition is applied all possible required tests. You can derive tests using any method you like but list your tests in the table below which requires you to list and check the inputs and outputs of each partition for each test. Note that you may not need as many vectors as the space provided in the table. Also, some of the column headings repeat to make the checking easier, but these columns must have identical entries to be consistent.

Test #	A	B	F	C	D	G	H	D	E	I	H	J
1	0	0	0	1	0	0	1	0	1	1	1	1
2	0	1	1	0	1	0	0	1	0	1	0	0
3	1	0	1	1	1	1	1	1	0	1	1	1
4	1	1	0	0	0	1	0	0	x	1	0	0
5								1	1	0	1	
6								1	1	0	0	
7								0	0			

In the table I have written test as follows. —— First four apply all 4 tests to all EOR and ENOR gates while their outputs are sensitized to J. This requires the I input to the gate J to be 1. While doing this I chose the inputs D and E such that two tests are also applied to gate I when gate H is 1.

I notice that during this time only two of the four tests are applied to gate J. Hence next the inputs can be chosen such that two additional tests are applied to gate J. Once again I choose D and E such that when H is 1, an additional test is also applied to gate I.

Finally, we need to apply one test to gate I while choosing inputs such that H is 1.

As a result I left many entries blank - these can be filled by simply working your way back.

7. (**16 points**) **DFT: Full and Partial Scan**

   Specifications of a large sequential circuit are given below:

```
Number of PIs          102       Number of POs          129
Number of FFs          1602     Number of gates        490,455
```

   This circuit is designed to operate at 2 GHz (500 picoSec clock period). However due to test time issues, the following full and partial scan DFT methods are candidates to ease the test problem. The impact of the DFT and other relevant details are given below.

```
No Scan: No change in performance. The test generator generates 50,050,075
sequential vectors and provides 90.5% fault efficiency.

Partial Scan: By placing 525 FFs in the scan path, the test generator
generates 20,900 vectors and provides 98.75% fault efficiency.
However the system performance degrades by 10% and as a result the
system operates at 550 picoSec clock.

Full Scan: By placing all FFs in the scan path, the test generator
generates 2,100 vectors for 100% fault efficiency. However the system
performance degrades same as for partial scan, i.e. 550 picoSec system clock.
Further, to keep the area overhead small, the scan related signals
are not well conditioned and therefore the scan operation for full
scan can run no faster than 1000 picoSec per scan shift operation.
```

   (a) (**1 point**) If partial scan DFT method is used, do we need any modification to the non-scan flip-flops? Explain in no more than 15 words.

   Yes. The non scan FFs should be modified in a way that during scan operation, they hold their values.

   (b) (**1 point**) What is number of primary inputs and primary outputs for test generation purposes for no scan environment?

   Number of PIs = 102
   Number of POs = 129

   (c) (**1 points**) What is number of primary inputs and primary outputs for test generation purposes for partial scan environment?

   Number of PIs = 102 + 525 = 627
   Number of POs = 129 + 525 = 654

(d) (**1 points**) What is number of primary inputs and primary outputs for test generation purposes for full scan environment?

Number of PIs = 102 + 1602 = 1704
Number of POs = 129 + 1602 = 1731

(e) (**2 points**) Compute the number of system clocks and the test application time in **milliseconds** for testing the circuit with no scan. Show your work.

Number of system clocks = 50,050,075
Test time = 25.025 milliseconds
Note: 500 picoseconds is 0.5×10^{-6} **milliseconds**.

(f) (**4 points**) Compute the number of scan clocks, system clocks, and test application time, in **milliseconds**, for testing the circuit with partial scan. You are not required to test the scan chain. Show your work.

Number of scan clocks = $525 \times 20,900 \; + \; 525$ = 10,973,025
Number of system clocks = 20.900
Test time = $10,973,025 \times 0.55 \times 10^{-6} \; + \; 20,900 \times 0.55 \times 10^{-6}$
= 6.035 + 0.011 = 6.045 milliseconds

(g) (**4 points**) Compute the number of scan clocks, system clocks, and test application time, in **milliseconds**, for testing the circuit with full scan. You are not required to test the scan chain. Show your work.

Number of scan clocks = $1,602 \times 2,100 \; + \; 1,602$ = 3,365,802
Number of system clocks = 20.900
Test time = $3,365,802 \times 1.0 \times 10^{-6} \; + \; 20,900 \times 0.55 \times 10^{-6}$
= 3.366 + 0.002 = 3.368 milliseconds

(h) (**2 points**) Comment on the method you would recommend to use to test this circuit. Give one or two solid reasons only.

Any method can be justified if no cost function is given. Important thing is to give two good reasons.

For example, I can justify Full Scan using the following argument. It offers 1) highest fault coverage and 2) relative to partial scan the test time is reduced substantially but the performance degradation is same as partial scan.

8. (**12 points**) **BIST**

Consider a characteristic polynomial

$$x^4 + x + 1$$

Now answer the following and you must show your work for full credit.

(a) (**4 points**) Is this polynomial factorable? If it can not be factored you must prove it and if it can be factored you should provide its factors.

No, this can not be factored. To prove it we need to divide with all possible non-factorable polynomials of degree two. These are x, $x+1$, and x^2+x+1.
If divided by x the remainder will be 1.
If divided by $x+1$ the remainder will be 1.
If divided by x^2+x+1 the remainder will be 1.
In none these cases remainder is 0, there for it can not be factored.

(b) (**2 points**) Give an internal exclusive-OR (modular) realization of this polynomial. For your convenience I have already drawn four FFs in the figure 6 below. (DATA input shown refers to part d)

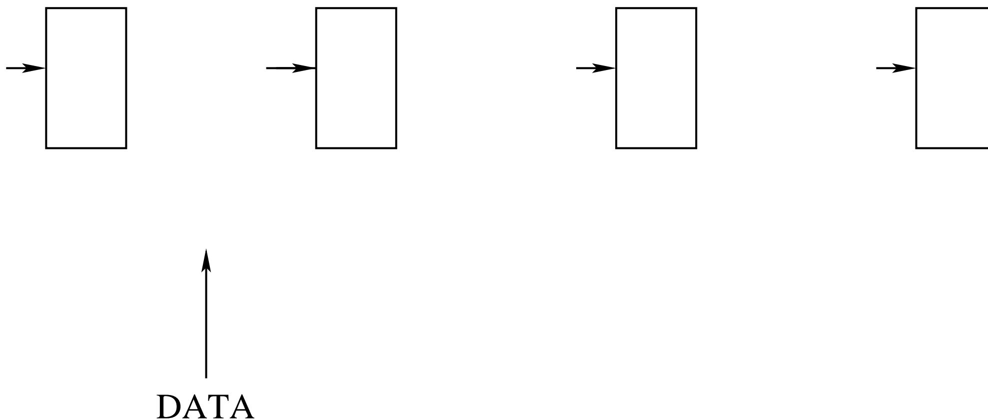

Figure 6: A modular linear feedback shift register

The realization is given in figure 7

(c) (**2 points**) A data sequence is to be fed to this LFSR. The data sequence is

`0 1 0 0 1 1 0 0 1`

with the most significant bit written on the left and the least significant bit to the right. Write this sequence in the polynomial form.

The polynomial representation is:

$$x^7 + x^4 + x^3 + 1$$

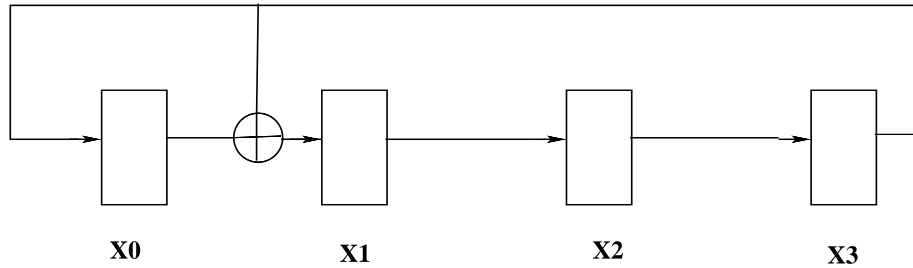

Figure 7: A modular linear feedback shift register realization

(d) (**4 points**) The sequence above is fed to a modular realization of MISR with the characteristic polynomial $x^4 + x + 1$. The location where the sequence is fed is marked as **DATA** in the figure 6. Determine the signature (contents of MISR) of the circuit producing this sequence as output. You must use the method of polynomial division and show your work.

For using algebraic method we fist have to move the DATA to the left most position. This is equivalent to multiplying the DATA polynomial by x.
Hence the polynomial to be divided will be $x^8+x^5+x^4+x$. Now divide this by x^4+x+1 and we obtain a remainder of x.
Answer The signature in polynomial form is: x
This if written as a bit sequence using the notation consistent with the external LFSR labeling (which labels the MSB to the right) will be will be 0100. You can verify this by simulation.

9. (**9 points**) **Boundary scan and general problems**

A board contains five ICs all of which have boundary scan. The information about these ICs is given in the table below:

Device information	IC-1	IC-2	IC-3	IC-4	IC-5
Number of input pins	211	210	198	175	150
Number of output pins	251	175	129	175	150
Number of bidirectional pins	0	5	0	45	0
Number of three state pins	15	5	0	57	90
Number of POWER pins	51	75	129	105	110
Number of GROUND pins	51	75	129	105	110
Bits in Instruction reg	4	3	5	3	7
Bits in Device ID reg	45	45	52	50	45

Answer the following:

(a) (**1 points**) How many extra pins does each device needed to have relative to non-boundary scan environment?

4 pins. However, a vendor chooses, it can also provide the 5th optional pin.

(b) (**1 points**) What is the length of Boundary scan data register (number of flip-flops in the boundary scan) for the IC-1?

211 + 251 + 2x15 = 492

(c) (**1 points**) What is the length of Boundary scan data register (number of flip-flops in the boundary scan) for the IC-2?

210 + 175 + 3x5 + 2x5 = 410

(d) (**1 points**) What is the length of Boundary scan data register (number of flip-flops in the boundary scan) for the IC-3?

198 + 129 = 327

(e) (**2 points**) Assuming that the TAP controller on each ICs is in Shift-DR state, after configuring each device into Device ID register read mode, how many test clocks (TCK) are required to read out the device ID of all five devices?

45 + 45 + 52 + 50 + 45 = 237

(f) (**2 points**) Assume that IC-1, IC-2, IC-3 and IC-4 are in bypass modes and the TAP controller on each ICs is in Shift-DR state, how many test clocks (TCK) are required to load the boundary register of IC-5? You can assume that the ICs are connected in sequential order.

4 + 150 + 150 + 2x90 = 484

(g) (**1 points**) Are the power and ground pins placed in the boundary scan data register?

No. Power and ground pins are not in the boundary scan path.