

**Department of Electrical and Computer Engineering
University of Wisconsin–Madison**

ECE 553: Testing and Testable Design of Digital Systems
Fall 2010-2011

Midterm Examination

SOLUTION

CLOSED BOOK

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Date: November 11, 2010
Place: Room 1164 Mechanical Engineering (Class location)
Time: 7:15 - 8:30 PM
Duration: 75 minutes

PROBLEM	TOPIC	POINTS	SCORE
1	General Questions	10	
2	Test Economics	12	
3	Modeling	13	
4	Fault Modeling	12	
5	Fault Simulation	12	
6	SCOAP Computation	10	
7	Test Generation - Comb	12	
8	Test Generation - Seq	10	
9	Checking Seq	9	
TOTAL		100	

Show your work carefully for both full and partial credit.
You will be given credit only for what appears on your exam.

Last Name (Please print): **SOLUTION** _____

First Name: _____

ID Number: _____

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1. (10 points) General Questions

Answer the following in brief and to the point.

- (a) (1 points) What defect model is used to derive the yield equation in the paper by William and Brown included in the reading material?

Random defects

- (b) (1 points) Name one forward time sequential test generator.

Fastest

- (c) (1 points) Name one reverse time sequential test generator.

There are many - HITEST is an example discussed in the paper

- (d) (1 points) Name one simulation based sequential test generator.

CONTEST - one of the example mentioned in the paper

- (e) (2 points) Should redundancy always be removed from a circuit? Explain.

From design point of view it may be desirable in some cases as in fault tolerant designs.

- (f) (2 points) Name two techniques that can be used to reduce the number of test patterns for a combinational circuit while still providing the same or better fault coverage.

Fault list reduction: fault equivalence, fault dominance, ...

Compaction: Static compaction, Dynamic compaction, reserve order simulation ..

- (g) (1 points) Is the claim that concurrent fault simulator in general require larger memory than deductive fault simulator, true?

Yes. The fault lists associated with a gate in deductive fault simulation are subset of the lists associated in concurrent fault simulation.

- (h) (1 points) Is it possible for a circuit to have a Distinguishing sequence but not have a synchronizing sequence?

Yes. A simple example is a modulo k counter without reset.

2. (12 points) Test Economics

While answering the following you must show your work. A Manufacturer of an IC performs two types of tests on its product.

(a) **(6 points)** The type 1 test is for *defect testing* to sort out defective devices from the good devices. Based on its fabrication line and experience, the manufacturer has found that 96% fault coverage is sufficient for the IC manufactured by it. The area of the IC is 0.60 sq. cm., the fault density is 1.5 faults/sq. cm., and the fault clustering factor β is 0.15.

i. **(3 points)** What is the Yield of the type 1 test that performs *defect testing*?
Using the Yield equation

$$Y(T) = \left(1 + \frac{Taf}{\beta}\right)^{-\beta}$$

and substituting $T = 0.96$, $a = 0.6$, $f = 1.5$ and $\beta = 0.15$
we get $Y = 0.7507$

ii. **(3 points)** What is the defect level in the devices that pass type 1 test performed for *defect testing*?
Using the equation for Defect level

$$DL = 1 - \left(\frac{\beta + Taf}{\beta + Af}\right)^{\beta}$$

and substituting $T = 0.96$, $a = 0.6$, $f = 1.5$ and $\beta = 0.15$
we get $DL = 0.00522$, i.e. 5220 ppm

(b) **(4 points)** The type 2 test is performed only on the ICs which pass the type 1 test, i.e. are expected to be defect free. This test is for *speed binning*. The objective here is to divide all the ICs into two bins, *fast bin* and *slow bin*. Devices which are in the fast bin can run at 1.5 GHz or more (faster ICs) and are sold at higher price relative to the devices which are in slow bin (slower ICs). The following information is given about this testing stage. Of all the devices that passed *defect test* it is known that 30% of them are truly fast and 70% of them are truly slow. However the *speed binning* test is not perfect and the Figure 1 below gives different probabilities for a device to be in the fast or slow bin.

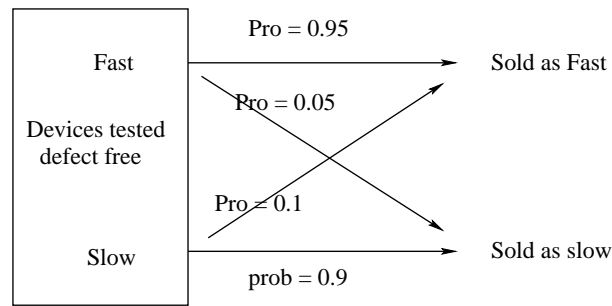


Figure 1: A Speed Binning Test

- i. **(3 points)** The devices that are tested by type 2 test, what percentage of those will appear in the *fast bin*?

The percentage of all devices that are tested by type 2 test and which will appear in the fast bin is

$$(0.3 \times 0.95 + 0.7 \times 0.1) \times 100 = 35.5$$

- (c) **(3 points)** What is the max percentage of devices that are sold as fast, are likely to be returned as either slow devices or defective devices. You can assume that type 2 test is unable to perform defect testing and defective devices that pass the type 1 test are uniformly distributed.

The percentage of slow devices in the fast bin is $(0.07 \times 100) / .355 = 19.718\%$

The percentage of fast defective devices in the fast bin due limited ability of type 1 test is $100 \times 0.00522 (.355 - .07) / 0.355 = 0.419$

Hence the percentage of return will be $19.718 + 0.419 = 20.137$

Note: This takes into account the slow devices that are defective. Hence is a tight bound.

3. (13 points) Modeling

Consider a combinational functional block with three inputs, A, B, and C, and two outputs, f_1 and f_2 . The model of this block in the form of a truth table is given below:

A	B	C	f_1	f_2
0	0	0	0	1
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	0	0
1	1	0	1	1
1	1	1	0	1

- (a) (2 points) Write a singular cover of the function f_1 .
 001/1; 1x0/1; 0x0/0; 1x1/0; x11/0 or 01x/0;
- (b) (2 points) Write the ordered BDD of the function f_2 assuming the order of variables to be A, C, B. **Note:** do not write reduced OBDD and pay attention to the order of variable while writing your answer.
 See Figure 2 below. (the figure has a typographical error)

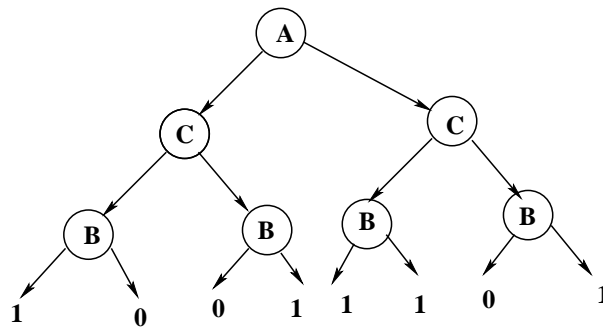


Figure 2: Ordered BDD

- (c) (**2 points**) Find one propagation D cube that will propagate a D at the input A to the output f_1 only and not to the output f_2 . **Note:** When a D propagates, the output can be either D or \overline{D} .

There are exactly three cubes which propagate D on A to output(s). These are:

$$D00/D1; \quad D01/\overline{D}0; \quad D10/DD$$

Hence any one of the first two is correct answer.

- (d) (**2 points**) Find one propagation D cube that will propagate a D at the input C to the output f_2 only and not to the output f_1 .

There are exactly four cubes which propagate D on C to output(s). These are:

$$00D/DD\overline{D}; \quad 01D/0D; \quad 10D/\overline{D}\overline{D}; \quad 11D/\overline{D}1$$

Hence the correct answer is second cube in the above list.

- (e) (**2 points**) Find one propagation D cube that will propagate a \overline{D} at the input B to both the outputs f_1 and f_2 . **Note:** When a \overline{D} propagates, the output can be either D or \overline{D} .

There are exactly two cubes which propagate \overline{D} on B to output(s). These are:

$$0\overline{D}1/DD\overline{D}; \quad 1\overline{D}1/0\overline{D}$$

Hence the correct answer is the first cube in the above list.

(f) (3 points) Netlist description of a sequential circuit is given below. Draw the circuit.

```

1  PI    3, 5 ;
2  PI    4 ;
3  NOT   4 ;
4  NAND  6, 7 ;
5  NAND  6 ;
6  NAND  8 ;
7  NOT   9 ;
8  FF    5 ;
9  PO
    
```

The circuit is given in Figure 3 below.

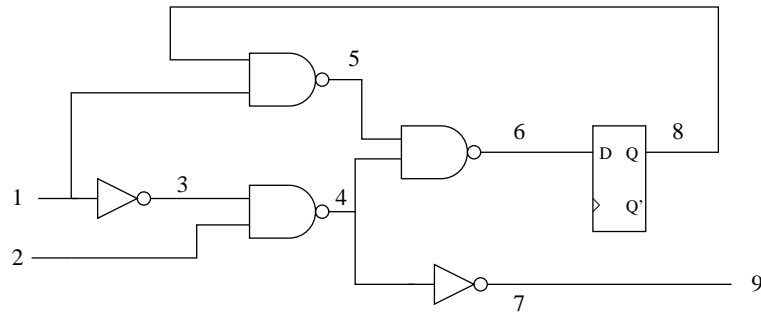


Figure 3: Circuit obtained from the netlist description

4. (12 points) Fault Modeling

Consider a fanout free combinational circuit given in Figure 4 below. Note this circuit has a total of 12 fault sites (A through L) and all lines in the circuits have been labeled.

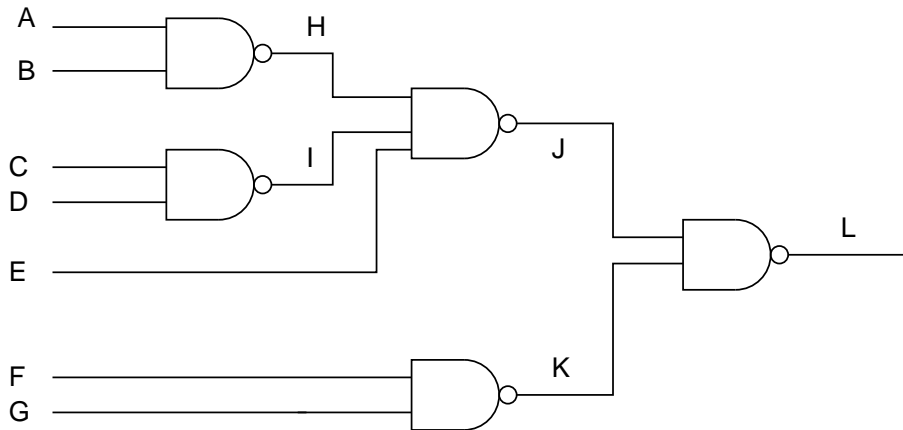


Figure 4: A Fanout Free Circuit

- (a) (1 points) What is the total number of single stuck at faults in this circuit?

There are 24 stuck-at faults

- (b) (6 points) In the table below list all single stuck-at faults after using the equivalence fault reduction method. In the column under *Rep. fault* write one fault that you chose as a representative of the equivalent fault set and following that in the same row write remaining faults that are equivalent to it. The table contains more entries than what you may need. I have completed one full entry of the table for you.

Num	Rep. Fault	Equivalent faults	Num	Rep. Fault	Equivalent faults
1	A/0	B/0, H/1	2	A/1	
3	B/1		4	C/0	D/0, I/1
5	C/1		6	D/1	
7	E/0	H/0, I/0, J/1	8	E/1	
9	F/0	G/0, K/1	10	F/1	
11	G/1		12	J/0	K/0, L/1
13	L/0		14		
15			16		
17			18		

(c) (1 points) How many checkpoints does this circuit have?

Number of checkpoints = 7; For a fanout free circuit the only checkpoints are Primary Inputs.

(d) (4 points) What will be the reduced number of faults using the method of checkpoint faults and then using fault equivalence reduction. Provide the reduced fault list.

Reduced fault list will be:

A/0, A/1, B/1, C/0, C/1, D/1, E/0, E/1, F/0, F/1, G/1

Hence the number of faults will be 11.

5. (12 points) Fault Simulation - Deductive

- Part of a very large circuit is reproduced in Figure 5 below. The faults of interests are
- 1) stuck at faults on the lines labeled between L1 .. L12; and
 - 2) a/0, b/1, c/0, d/1, e/1, and f/1 in the remaining circuit that is not shown.

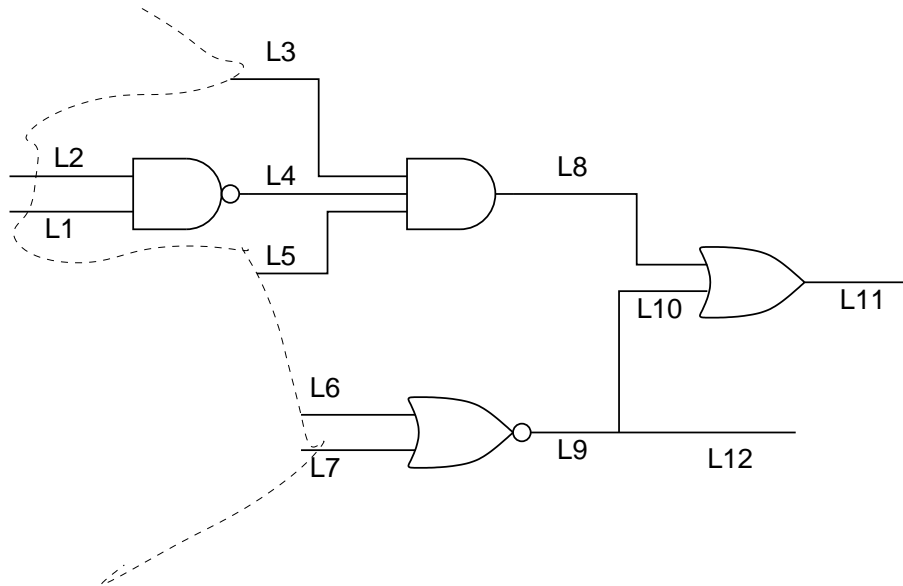


Figure 5: Circuit for Deductive Fault Simulation

In the table below, the first three columns contain the line labels, some of the signal values, and partial fault lists obtained using deductive fault simulation techniques. You are to complete the last two columns of the table by filling in all the signal values and complete deductive fault list associated with each line. But you are to use only deductive reasoning. If some data is missing that means deductive reasoning does not lead to any information about the missing data.

Line	Info Provided		Your Deduced Answers	
	Sig value	Partial List	Sig value	List
L1	0	a/0, b/1, c/0, f/1, L1/1	0	no change
L2		b/1, L2/0	1	no change
L3	1	d/1, L3/0	1	no change
L4			1	a/0, c/0, f/1, L1/1, L4/0
L5	0	c/0, e/1	0	c/0, e/1, L5/1
L6		L6/0, e/1	1	no change
L7	0	a/0, b/1	0	a/0, b/1, L7/1
L8			0	e/1, L5/1, L8/1
L9			0	e/1, L6/0, L9/1
L10			0	e/1, L6/0, L9/1, L10/1
L11			0	e/1, L6/0, L9/1, L10/1, L5/1, L8/1, L11/1
L12			0	e/1, L6/0, L9/1, L12/1

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6. (10 points) **SCOAP Computation**

Consider the circuit given in Figure 6 You are to compute the SCOAP controllability

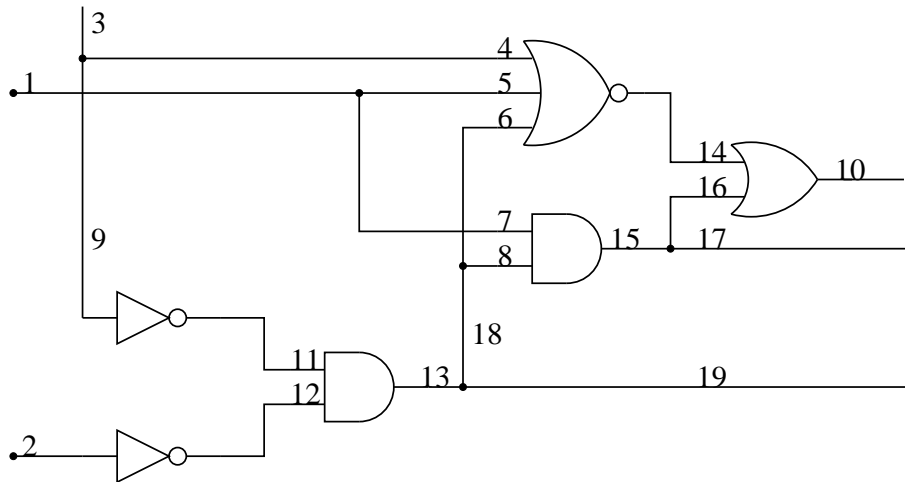


Figure 6: Circuit for SCOAP computations

values of the lines in the circuit that are specified in the table below. I have completed some of the entries for this circuit that will help you calculate the remaining entries.

Line	CC0	CC1	Line	CC0	CC1	Line	CC0	CC1
1	50	35	2	27	44	3	10	5
4	10	5	5	50	35	6	7	40
7	50	35	8	7	40	9	10	5
10	15	69	11	6	11	12	45	28
13	7	40	14	6	68	15	8	76
16	8	76	17	8	76	18	7	40
19	7	40						

7. (12 points) Combinational Test Generation - PODEM

A PODEM like test generator is used to generate a test for the fault w s-a-1 in the circuit below. This test generator has a priority decided to choose the circuit primary inputs (PIs) for assignments in the following fixed order irrespective of the objective. The order of choosing inputs: B, A, E, C, D, F

Further, it always assigns the value 0 before assigning a value 1 to an input. This means, for example, if at some stage the PIs B, A and E have been assigned, then the next PI chosen will be the input C and it will be assigned a value 0. After assignment, it performs full implication. And, after each implication, if the objective can not be satisfied or there is no x-path from D-frontier to the output, it backtracks and complements the latest PI assignment that has not yet been complemented in the decision tree.

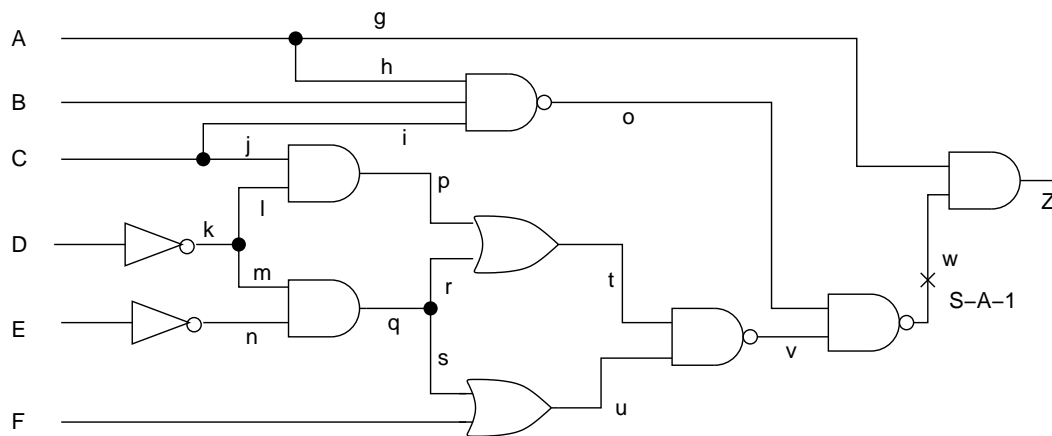


Figure 7: Circuit under test

- (a) (10 points) The table below contains completed two steps of the test generation process, including PI assignment, implications, and comments. Complete the test generation. Note, in the comment column, list the reason for proceeding forward or for backtrack.

Step No.	PI assign	Implication	comment
1	B=0	o=1	fault not excited
2	A=0	g=0 h=0 Z=0	Output constant: backtrack
3	A=1	g=1, h=1	fault not excited
4	E=0	n=1	fault not excited
5	C=0	i=0, j=0, p=0	fault not excited
6	D=0	k=1, l=1, m=1, q=1, r=1 s=1, t=1, u=1, v=0, w=1	fault can not be be excited, backtrack
7	D=1	k=0, l=0, m=0, q=0, r=0 s=0, t=0, v=1, w=0(\overline{D} , $Z=\overline{D}$)	test found
8			

- (b) (2 points) Draw the decision tree that will be created by the above test generator for the given fault.

Decision tree is given in Figure 8 below.

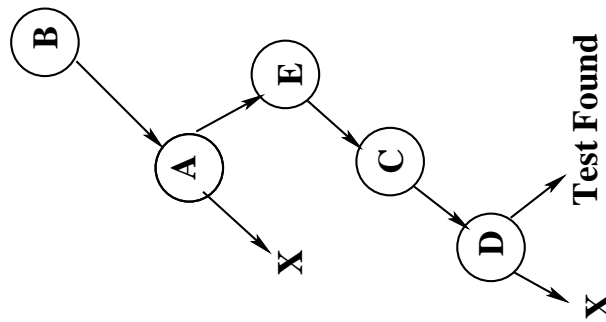


Figure 8: Decision Tree

8. (10 points) **Test Generation - Sequential**

Consider the sequential circuit given below in Figure 9 containing two D-type flip-flops and a logic gate.

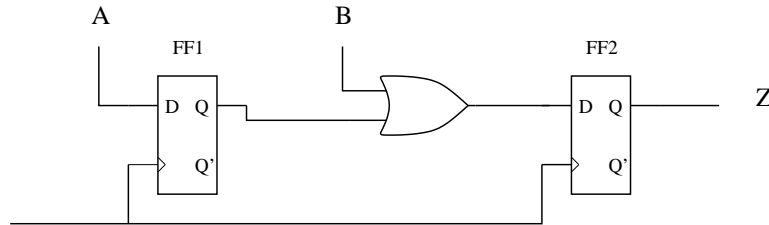


Figure 9: Figure for a sequential circuit

- (a) (2 points) In the figure 10 below I have provided two FFs and a box for the combinational part of the circuit. Redraw the combinational part of circuit in the box and make all the connections. Note the FF labels: FF2 is drawn above FF1.

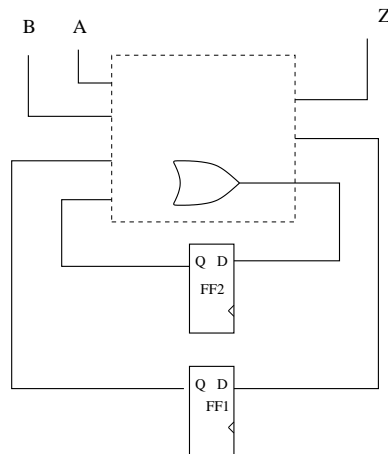


Figure 10: Figure for combinational part of the sequential circuit

The circuit within the block is in Figure 11

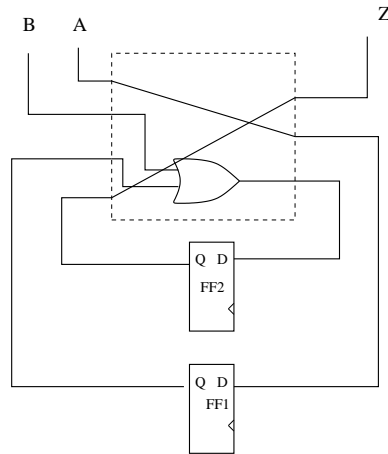


Figure 11: Figure for combinational part of the sequential circuit

- (b) (4 points) Draw the time frame expansion of this circuit for three time frames. Mark the inputs, outputs, pseudo primary inputs and pseudo primary outputs appropriately in the model you draw.

The timeframe expansion model is shown in Figure 12

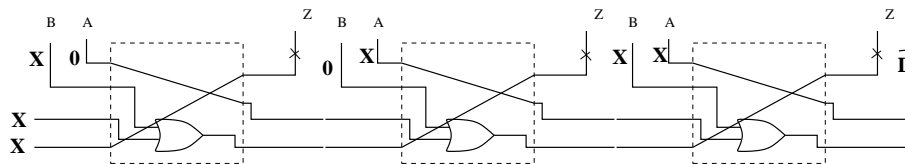


Figure 12: Time frame expansion of the sequential circuit

- (c) (4 points) Derive a test sequence that will detect the stuck-at 1 fault at the output Z. You can use any method you like. Use the time frame expansion drawn by you to show clearly the values of the inputs and the time the values are applied. You must also indicate the time the fault is detected and what will be the expected output and the output of the faulty circuit for the input sequence obtained by you.

The input sequence will be $AB(t=1) 0X$, $AB(t=2) X0$, $AB(t=3) XX$

The fault will be detected after application of second clock, i.e. in the third timeframe. The output will be \overline{D} , i.e. expected output is 0 and faulty circuit will produce a 1.

9. (9 points) Checking Experiment

State table of a finite state machine with five states, A, B, C, D, E; and an input alphabet consisting of a, b, c, d; is given below. Answer the questions below, and you **must show your work otherwise no points** will be awarded.

Table 1: State Machine for Problem 7

	Input			
	a	b	c	d
A	A/0	E/1	B/1	C/0
B	B/0	B/0	B/0	D/0
C	C/1	D/1	E/0	A/1
D	D/0	C/0	A/1	E/1
E	E/0	A/1	E/1	A/1

- (a) **(3 points)** Is the sequence “b c d c” a distinguishing sequence for this circuit? You must show your work and a yes/no answer will not be given any points.

There are two ways to confirm this. 1) To check the output seq for every start state and show that they are all distinct. 2) To proceed on the same lines as distinguishing tree to show that all states can be distinguished by this sequence. The second method is shown below:

```
(ABCDE)
 | b
(BC) (ADE)
 | c
(BE) (ABE)
 | d
(D) (A) (CD) (A)
 | c
(A) (B) (E) (A) (B)
```

- (b) (2 points) If the sequence “a b c d c” is applied to the above circuit when the circuit is in state A, what will be the output sequence and the final state of this circuit?

The output sequence and the state sequence that will result is shown below:

input		a	b	c	d	c
states	A	A	E	E	A	B
outputs		0	1	1	1	1

- (c) (4 points) Find a shortest possible *synchronizing sequence* for the above finite state machine.

We can construct a synchronizing tree.

A shortest synchronizing sequence is: c c b c

(Note: you can reduce your work by realizing the input a never changes the state ambiguity at any stage, therefore it can not be part of a shortest synchronizing sequence) Figure /refsynchro-tree shows the derivation of the sequence.

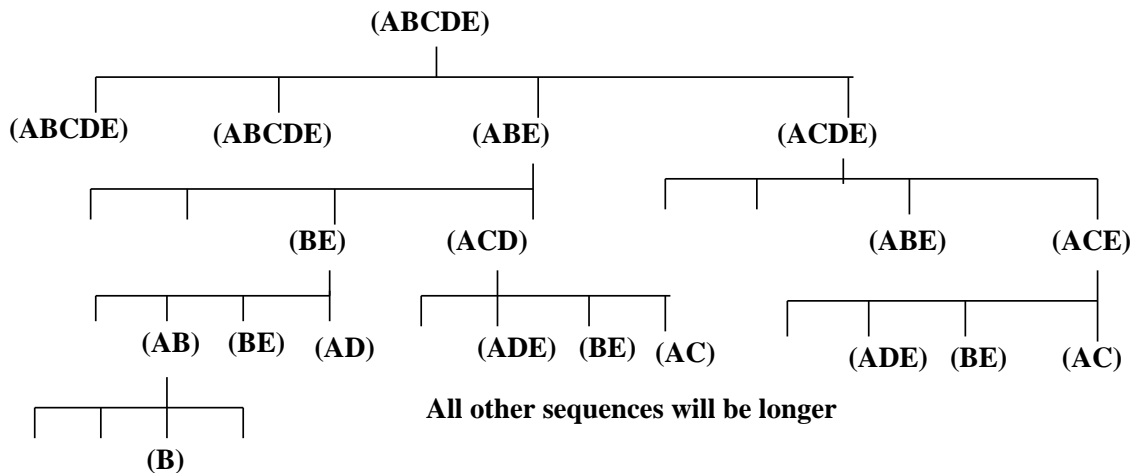


Figure 13: Synchronizing Tree