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Department of Electrical and Computer Engineering
University of Wisconsin–Madison

ECE 553: Testing and Testable Design of Digital Systems
Fall 2011-2012

Midterm Examination

CLOSED BOOK

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Date: November 10, 2011
Place: Room 1153 Mechanical Engineering
Time: 7:15 - 8:55 PM
Duration: 100 minutes

PROBLEM	TOPIC	POINTS	SCORE
1	General Questions	10	
2	Test Economics	15	
3	Logic and Fault Modeling	14	
4	Fault Simulation	13	
5	SCOAP Computation	10	
6	Test Generation - Comb.	16	
7	Test Generation - Seq.	10	
8	Checking Sequence	12	
TOTAL		100	

Show your work carefully for both full and partial credit.
You will be given credit only for what appears on your exam.

Last Name (Please print): **SOLUTION** ____________
First Name: ______________________
ID Number: ______________________

1. (**10 points**) **General Questions**

   Answer the following in brief and to the point.

   (a) (**1 points**) Give one reason as to why a circuit that is tested good may fail when a customer uses it.

   Less than 100% fault coverage
   Presence of faults not modeled by the fault model
   ...

   (b) (**1 points**) What defect model is used to derive the yield equation in the paper by William and Brown included in the reading material?

   Random defects

   (c) (**1 points**) If a fault f_1 is equivalent to f_2 and the fault f_1 dominates a fault f_3, then which of these fault or faults can be deleted to reduce the the fault list for the purpose of fault detection. Give reason.

   Only f_3 needs to be kept. Fault f_1 is equivalent to f_2, therefor we can remove either one of them. In particular we can delete f_2. Next f_1 dominates f_3, therefore we can delete f_1.

   (d) (**2 points**) A single output combinational circuit is simulated using 3-value logic with some inputs specified (0s and 1s) while other inputs not specified (Xs). The output of the circuit is found to be a constant (0 or 1). Prove by proper reasoning or by an example that for the same input values and in the presence of a stuck-at fault in the circuit the output can be X. Use only the space provided.

   A simple example will be to consider a NAND with two inputs A and B. For A =0 and B = X, the output will be 1. Now in the presence of a fault A s-at-1 the faulty gate will produce and output X.

   (e) (**1 points**) A test algorithm which is capable of finding all tests for a fault in a combinational circuit can determine if a given fault in the circuit is redundant. Answer True or False.

   True

(f) (**1 points**) If the SCOAP CC0 value of a line in a circuit is 23, then using appropriate input assignment we can always set this line to logic 0. Answer True to False.

False

(g) (**1 points**) Circuits which have high fault coverage using Random Patterns are called
Random Pattern ...**Testable** ... Circuits.

(h) (**1 points**) Define *fault efficiency*.

$$\frac{No.\ of\ detected\ faults}{Total\ No.\ of\ faults - No.\ of\ undetectable\ faults}$$

(i) (**1 points**) Is it possible for a circuit to have a Synchronizing Sequence but not have a Homing Sequence? Explain your answer.

No. In the worst case synchronizing Sequence will work like a Homing Sequence.

2. (**15 points**) **Test Economics**

   Product details and process parameters of an IC being designed and fabricated by a Manufacturer are as follow:

   Area of the IC = 0.75 sq cm.
   Fault density f = 1.45 faults/sq cm
   Clustering factor $\beta = 0.11$
   Cost of producing a chip = $ 0.75 (note this is the cost of producing each chip before it is tested
   A chip that is tested good will be sold for $ 4.00
   Cost of replacing a bad chip = $ 15.00 You need not worry about the cost of test equipment and the length of the tests.

   The manufacturer of the IC can use one of the two tests which are available.
   1) Test T_1 provides a fault coverage of 90% and
   2) Test T_2 provides a fault coverage of 95%.

   The manufacturer wishes to produce 1 million chips for selling i.e. after testing the manufacturer would like to have 1 million devices that are tested "good".

   Now answer the following and while answering you must show your work.

   (a) (**3 points**) Determine the yields of the two tests.

   Using the Yield equation

   $$Y(T) = \left(1 + \frac{Taf}{\beta}\right)^{-\beta}$$

   and substituting $T_1 = 0.90$, A = 075., f = 1.45 and $\beta = 0.11$
   we get $Y(T_1) = 0.777125$
   Similarly for $T_2 = 0.95$ we get $Y(T_2) = 0.772970$.

(b) (**3 points**) Determine the defect levels for the devices tested by the tests T_1 and T_2 and express it in ppm (**parts per million**).

Using the equation for Defect level $DL = 1 - \left(\frac{\beta+Taf}{\beta+Af}\right)^{\beta}$ and substituting T_1T = 0.90, A = 0.75, f = 1.45 and $\beta = 0.11$
we get $DL(T_1) = 0.01042$, i.e. 10420 ppm

Similarly for the test $T_2 = 0.95$ we obtain $DL(T_2) = 0.005099$, i.e. 5099 ppm

You can also obtain the same results by computing $Y(1) = 0.76903$ and then use the equation $DL(T) = 1 - \frac{Y(1)}{Y(T)}$

(c) (**3 points**) For the test T_1 determine the cost of producing 1 million chips that well be sold, i.e. chips that are tested "good".

To produce 1 million good devices the number of devices that will have to be manufactured is $\frac{1\ million}{Yield}$. Thus the number of devices to be manufactured will be 1286793. Hence the cost will be 0.75x1286793 = $965094.75

(d) (**3 points**) For the chips tested by the test T_1 determine the total cost of replacing the bad chips.

The number of bad devices in the million devices will be $DL \times 1000000$. This is 10420. Hence the cost of replacing these will be $ 10420 = $ 156300.00

(e) (**3 points**) What will be the total profit for the chips tested by T_1.

Profit is 4000000 - 965095 - 156300 = $ 2,878,605.00

3. (**14 points**) **Logic and Fault Modeling**

   Consider a combinational functional block with three inputs, A, B, and C, and an output f. The model of this block in the form of a truth table is given below:

A	B	C	f	f_{fault}
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	1	1
1	1	1	0	0

   (a) (**2 points**) Write a singular cover of the function f.

   001/1; 1x0/1; 0x0/0; 1x1/0; x11/0 or 01x/0;

   (b) (**2 points**) Write two propagation D-cubes of the functional block realizing the function f and containing only one D at some input.

   There are many. Here are some examples.
   00D/D; Dx0/D; 11D/$\overline{D}$; 1xD/$\overline{D}$

   (c) (**2 points**) Write all D Cubes of failure of a fault that will cause the function f to change to the function f_{fault} as shown above.

   001/D; 101/$\overline{D}$

   (d) (**3 points**) Netlist description of a sequential circuit is given below. Draw the circuit.

```
1   PI     3, 5 ;
2   PI     5 ;
3   NOT    4 ;
4   NAND   6, 7 ;
5   NAND   6 ;
6   NAND   8 ;
```

```
8    FF      4 ;
7    PO
```

The circuit is given in Figure 1 below.

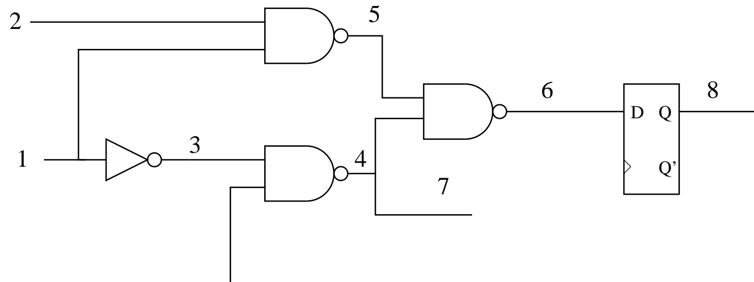

Figure 1: Circuit obtained from the netlist description

(e) (**5 points**) Consider a fanout free combinational circuit given below in Figure 2 and answer the questions related to this.

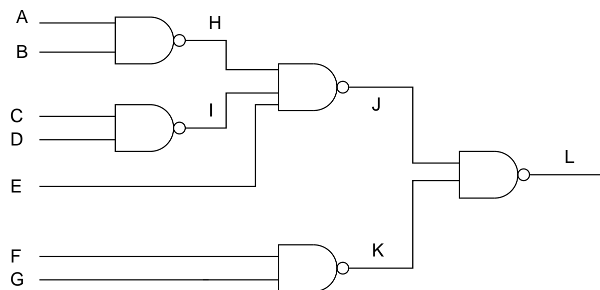

Figure 2: A Fanout Free Circuit

i. (**1 points**) How many checkpoints does this circuit have?

7 checkpoints

ii. (**1 points**) What will be the reduced number of faults using the method of checkpoint faults and then using fault equivalence reduction?

14 - 3 = 11 faults

iii. (**1 points**) If in the figure all NAND gates were replaced by NOR gates, what will be the number of reduced faults using checkpoint followed by equivalence reduction?

Same as above, i.e. 14-3 = 11 faults

iv. (**2 points**) If in the figure all NAND gates were replaced by AND gates, what will be the number of faults reduced by the method of fault equivalence?.

This will be a 7 input AND gate. Therefore the reduced number of faults will be:
if you reduce of checkpoints - 8
if reduced using only fault equivalence then 9.

4. (**13 points**) **Fault Simulation - Deductive**

The circuit of Figure 3 is to be simulated using the pattern given below:

```
pattern  =   A B C D E F  = 0 1 1 1 1 0
```

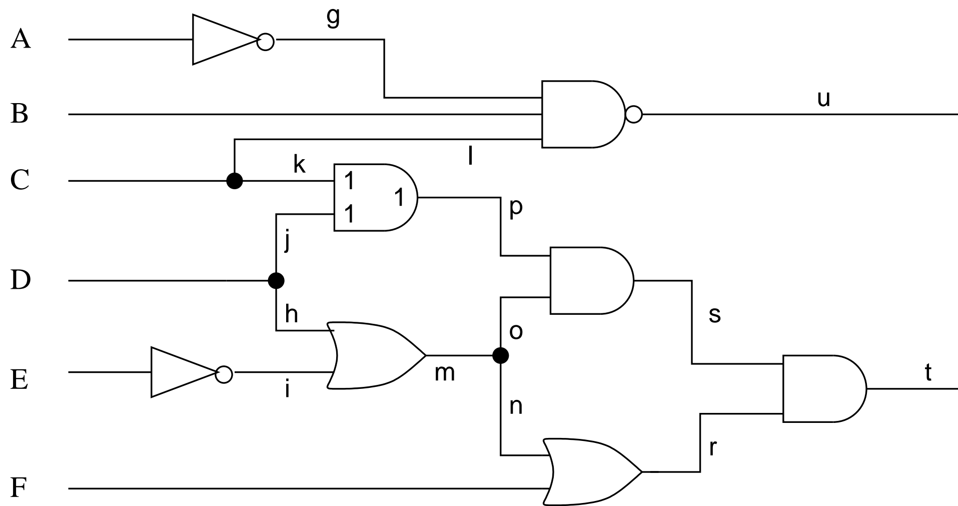

Figure 3: Circuit for deductive fault simulation

The fault list that needs to be simulated for this pattern is given below:

```
A/1  B/0  C/0  D/0  E/0  F/1  h/0  i/0  k/0 s/0
```

Note during deductive fault simulation the list associated with any line or gate should not contain a fault that is not in the above list.

(a) (**2 points**) Indicate the true signal values in every gate of the circuit. For your convenience, I have already provided values in one of the gates.

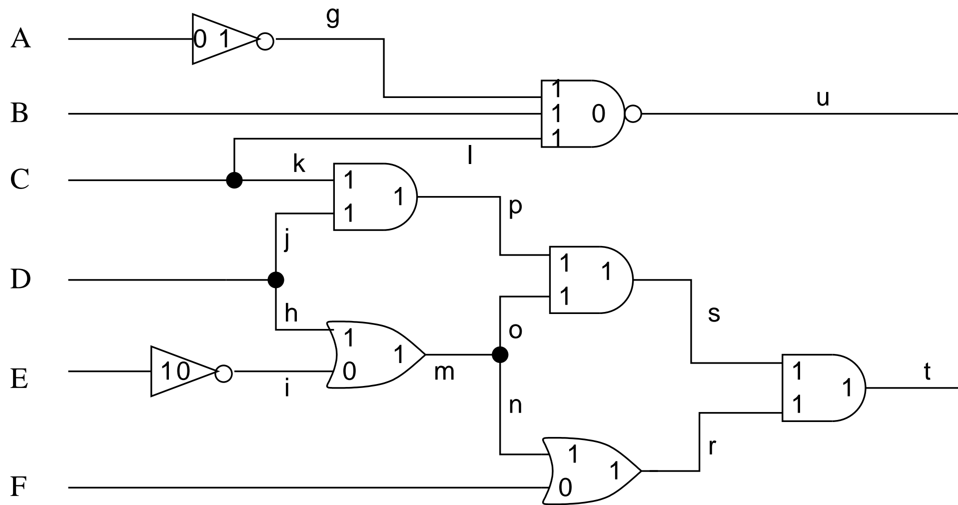

Figure 4: Circuit for deductive fault simulation with simulated values

(b) (**9 points**) In the table below provide the deductive fault list associated with every line in the circuit. Again to get you started, I have already completed the entries associated with all primary input lines.

Line Name	fault list	Line Name	fault list
A	A/1	l	C/0
B	B/0	m	D/0, h/0
C	C/0	n	D/0, h/0
D	D/0	o	D/0, h/0
E	E/0	p	D/0, C/0, k/0
F	F/1	r	D/0, h/0
g	A/1	s	D/0, h/0, C/0, k/0, s/0
h	D/0, h/0	t	C/0, D/0, h/0, k/0, s/0
i	E/0	u	B/0, A/1. C/0
j	D/0		
k	C/0, k/0		

(c) (**2 points**) Now, indicate which of the faults will be detected and at which output.

Faults detected at output u:

A/1, B/0, C/0

Faults detected at output t:

C/0, D/0, h/0, k/0, s/0

5. (**10 points**) **SCOAP Computation**

   Consider the two time frame expansion of a sequential circuit as given in the Figure 5 below. You are to compute the SCOAP controllability values of all the lines in the

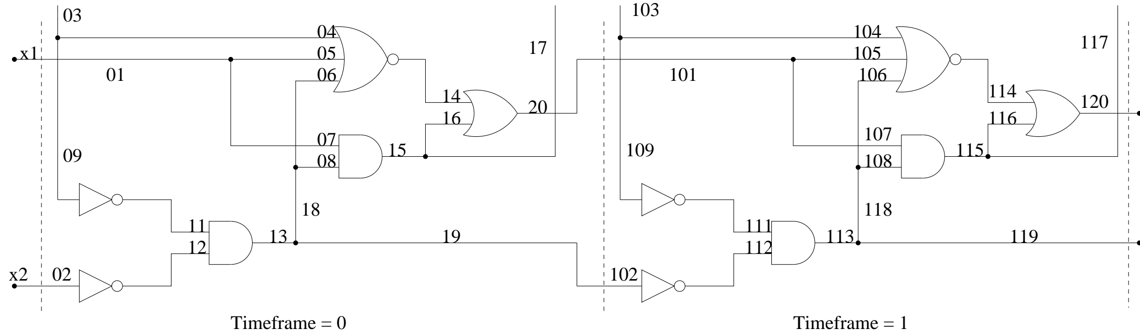

Figure 5: Circuit for SCOAP computations

   circuit in the table below. I have completed some of the entries for this circuit that will help you calculate the remaining entries. Use the rules given below for computing these values:

   (a) The (CC0, CC1) controllability values of all PIs (in any time frames) are (1, 1) as marked in the table below.

   (b) The (CC0, CC1) controllability values of the PPIs on the left are (∞, ∞) as marked in the table below.

   (c) The lines that cross time frame boundary, their CC0 and CC1 values get multiplied by 5, when they cross the time frame boundary.

Line	CC0	CC1	Line	CC0	CC1	Line	CC0	CC1
x1	∞	∞	x2	∞	∞			
01	∞	∞	02	∞	∞	03	1	1
04	1	1	05	∞	∞	06		
07	∞	∞	08			09	1	1
11	2	2	12			13		
14			15			16		
17			18			19		
20								
101			102			103	1	1
104	1	1	105			106		
107			108			109		
111	2	2	112			113		
114			115			116		
117			118			119		
120								

Completed table is given below.

Line	CC0	CC1	Line	CC0	CC1	Line	CC0	CC1
x1	∞	∞	x2	∞	∞			
01	∞	∞	02	∞	∞	03	1	1
04	1	1	05	∞	∞	06	3	∞
07	∞	∞	08	3	∞	09	1	1
11	2	2	12	∞	∞	13	3	∞
14	2	∞	15	4	∞	16	4	∞
17	4	∞	18	3	∞	19	3	∞
20	7	∞						
101	35	∞	102	15	∞	103	1	1
104	1	1	105	35	∞	106	3	19
107	35	∞	108	3	19	109	1	1
111	2	2	112	∞	16	113	3	19
114	2	40	115	4	∞	116	4	∞
117	4	∞	118	3	19	119	3	19
120	7	41						

6. (**16 points**) **Combinational Test Generation - PODEM**

A PODEM like test generator is used to generate a test for the line 13 s-a-0 in the circuit shown in Figure 6.

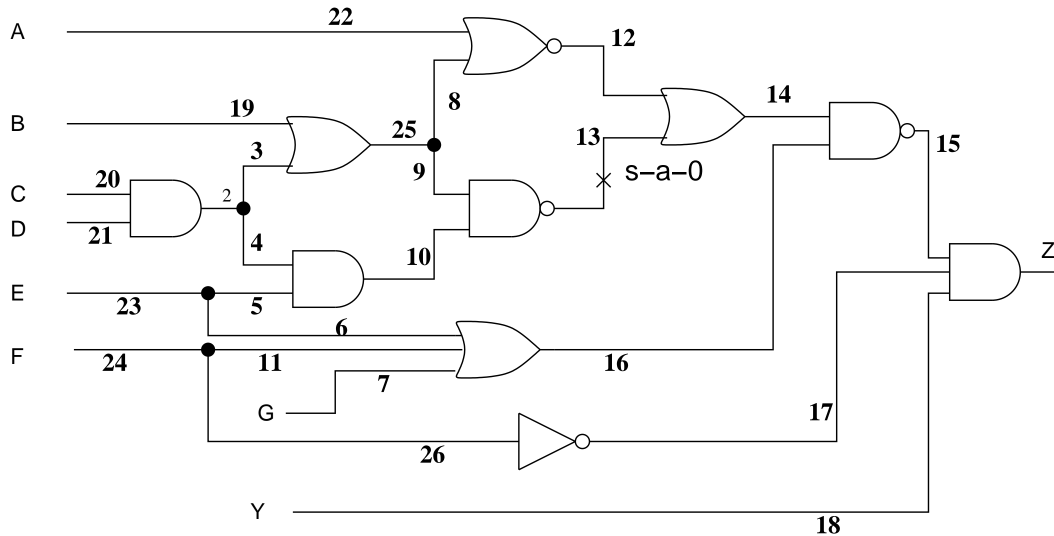

Figure 6: Combinational circuit for PODEM based test generation

In the table below part of the first three steps of the test generation process are shown. The following rules are used while using a PODEM like algorithm.

1) *While backtracing, whenever there is a choice between more than one paths, choose the one that contains a lower number label. For example if there is a choice between two paths labeled 9 and 10, follow the label 9.*

2) *While assigning a value at an input, always assign a* **0 before a 1**.

3) *Do not perform x-path check.*

Now answer the following.

(a) (**1 points**) Specify the backtrace path name in row 3.

(b) (**10 points**) Complete the rest of the test generation process but you must follow the rules given above. There are sufficiently many blank entries in the table to complete the test generation process.

(c) (**3 points**) Construct the decision tree for the complete test generation process for arriving at the final test or termination of the test process.

(d) (**2 points**) Write the generated test. A B C D E F G Y = 1 0 0 X 0 0 1 1

Step No.	Objec-tive	Name of the back-trace path	PI assign	D front	comment
1	13 to 0	13-9-25-3-2-20-C	C=0	-	fault not yet excited
2		13-9-25-19-B	B=0	14	fault excited
3	12 to 0	12-22-A	A=0	null	backtrack and reverse decision
4			A=1	15	
5	16 to 1	16-6-23–E	E=0	15	Objective not yet satisfied
6	16 to 1	16-7-G	G=0	15	Objective not yet satisfied
7	16 to 1	16-11-24-F	F=0	Null	Backtrack and reverse the decision
8			F=1	Null	Backtrack and reverse the decision G=0
9			G=1	Z	Note set F=x.
10	17 to 1	17-26-24-F	F=0	Z	
11	18 to 1	18-y	Y=0	Null	Back track and reverse the decision
12			Y=1		Success - Test found
13					

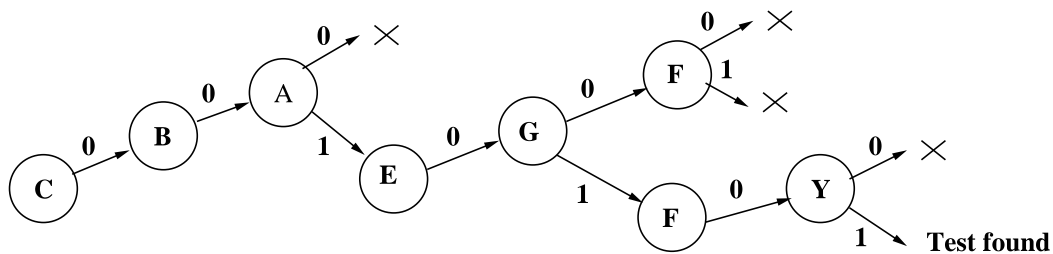

Figure 7: Decision Tree for PODEM based test generation

7. (**10 points**) **Test Generation - Sequential**

   Consider the sequential circuit given below in Figure 8 containing two D-type flip-flops and combinational logic. Note that the circuit has one primary input, A, and one primary output, Z.

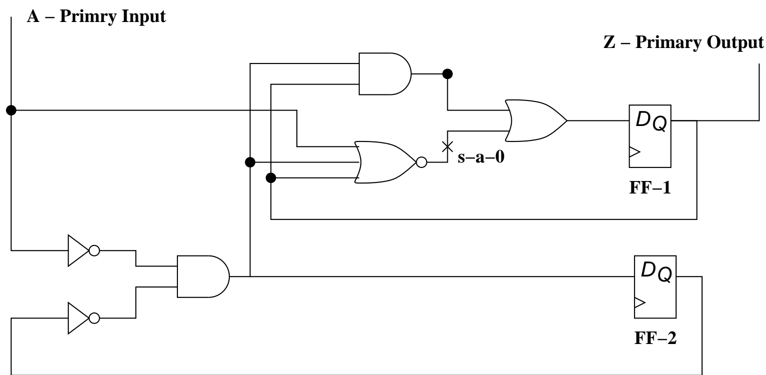

Figure 8: Figure for a sequential circuit

   Derive a test sequence that will detect the stuck-at 0 fault as shown in the circuit. You can use any method you like. For the sequence generated by you provide the following information in the tabular form given below which contains sufficiently many columns.

Initial state of the circuit - it should be XX
State of the fault-free and the faulty circuits after application of each clock
Output of the fault-free and the faulty circuit for each input
When is the fault excited and when is the fault detected.

		t = 0	t = 1	t = 2	t = 3	t = 4
Input A		A =	A =	A =	A =	A =
State (fault-free)	FF-1	X				
	FF-2	X				
fault-free Z						
State (faulty)	FF-1	X				
	FF-2	X				
faulty Z						

The test sequence is derived in the table below:

		t = 0	t = 1	t = 2	t = 3	t = 4
Input A		A = 1	A = 0	A = 0	A = X	A =
State (fault-free)	FF-1	X	0	0	1	
	FF-2	X	0	1	0	
fault-free Z		X	0	0	1	
State (faulty)	FF-1	X	0	0	0	
	FF-2	X	0	1	0	
faulty Z		X	0	0	0	

The fault will be excited at t = 2 and will be detected at t = 3.

8. (**129 points**) **Checking Experiment**

You are told that the finite state machine shown in the table with four states, A, B, C, and D; and one input has a Distinguishing sequence 0 0 0. Note that one of the next state entry is marked as * which needs to be determined.

Table 1: State Machine for Problem 7

	Input	
	0	1
A	*/0	C/0
B	C/0	D/0
C	A/0	B/0
D	D/1	A/1

Answer the questions below, and you **must show your work otherwise no points** will be awarded.

(a) (**6 points**) Determine the * entry (to be A, B, C,or D) so that the resulting finite state machine has 0 0 0 as a distinguishing sequence. You must explain the reason for your choice otherwise no points will be awarded.

1. The * entry can not be either A or C because both these are the next states with the output 0. The entry A will make the A and C to merge and hence indistinguishable if DS started with a 0. Similar reasoning for * not to be C.

2. If * is B then a 0 followed by a 0 will not lead to a shortest DS. Alternatively, it can be seen that 0 0 0 can not be a DS if * is B.

3. The only remaining possibility is * must be D. In this case we can verify that 0 0 0 is indeed a DS for this FSM.

(b) (**3 points**) Is the machine shown, without the knowledge about *, strongly connected? You must show your work and a yes/no answer will not be given any points.

Yes it is. One can check that we can go from any state (A,B,C, D) to any state without every going through *.

(c) (**3 points**) Find another *distinguishing sequence* for this finite state machine without the knowledge of * entry in the table.

A DS is 1 1 1