

**Department of Electrical and Computer Engineering
University of Wisconsin–Madison**

**ECE 553: Testing and Testable Design of Digital Systems
Fall 2009**

MIDTERM EXAMINATION - SYLLABUS

Date: **Monday**, November 9, 2009
Time: 7:15 PM **Evening exam**
Duration: 75 minutes
Location: Room 1164 Mechanical Engineering (class location)

The mid term examination will be held on November 9, 2009. It will be a 75 minutes examination. Although a *closed book* examination, you are allowed to bring a paper (cheat sheet) of size (8 1/2 × 11 inches) with you. You can write on it (both sides if you wish) what ever you think may assist you in the examination. You are also allowed to bring in a calculator of any kind. The total weight assigned to the examination is 25%.

You will be responsible for all the material covered in lectures till October 29 i.e. all material covered in the homework assignments 1, 2, 3, and 4. You are also expected to have read all the relevant papers from the set of notes. In summary you will be examined on the following contents of the course:

Introduction:

Introductory material. (Chapter 1)

VLSI Test Process:

How to test and types of tests. (Chapter 2)

Test Economics:

Test economics and yield issues.
(Chapter 3 and paper # 1)

Logic Modeling and Logic Simulation:

Different logic models discussed in class, Gate level simulation, 2 and 3 value simulation, compiled and table driven simulation, full and event directed simulation. (Lecture materials and Chapter 5)

Fault Modeling and Fault Simulation:

Fault modeling, fault list reduction, fault equivalence and dominance, redundancy and its removal. (Chapter 4) Serial, Parallel, deductive, concurrent, parallel pattern and parallel fault simulation. Sampling, and statistical fault analysis. (Chapter 5)

Test Generation:

Combinational logic - basic principles and basic methods, D-algorithm, and PODEM algorithms. ATPG system issues and solutions. (Chapter 7)

Testability Measures:

Purpose, origin, and SCOAP measure and its applications. (Chapter 6)

Sequential Circuit Test Generation:

Time frame expansion approach. FASTEST approach. Use of 9-value logic, forward, reverse and hybrid test generators. Simulation based approaches. Sequential ATPG systems. (Chapter 8 and paper # 2)

Functional Testing:

Checking experiment approach for sequential circuits (Papers # 3)