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**Department of Electrical and Computer Engineering
University of Wisconsin–Madison**

**ECE 553: Testing and Testable Design of Digital Systems
Fall 2011**

FINAL EXAMINATION - SYLLABUS

Date: **Saturday**, December 17, 2011
Time: 2:45 PM
Duration: 2 Hours
Location: Room 2540 Engineering Hall

The final examination will be held on the day, date, and time shown above. It will be a 2 hours examination to be held at the location specified above. Although a *closed book* examination, you are allowed to bring two papers (cheat sheets) of size (8 1/2 × 11 inches) with you. One from the midterm and the second you prepare for the final. You can write on both sides, if you wish, what ever you think may assist you in the final examination. You are also allowed to bring in a calculator of any kind. The total weight assigned to the examination is between 30 and 35%.

It will be a comprehensive examination and hence you will be responsible for all the material covered in class or assigned otherwise to be completed by you. Thus, you are expected to have read all the relevant papers which have been announced in class and are included in the set of notes. More weight will be given to the parts not covered by the midterm examination. You can expect a larger part (possibly nearly 60%) of the questions will be from the material not covered by the midterm examination.

In summary, you will be examined on the following contents of the course:

Introduction:

Introductory material. (Chapter 1)

VLSI Test Process:

How to test and types of tests. (Chapter 2)

Test Economics:

Test economics and yield issues.
(Chapter 3 and paper # 1)

Logic Modeling and Logic Simulation:

Different logic models discussed in class, Gate level simulation, 2 and 3 value simulation, compiled and table driven simulation, full and event directed simulation. (Lecture materials and Chapter 5)

Fault Modeling and Fault Simulation:

Fault modeling and fault list reduction. (Chapter 4)
Serial, Parallel, deductive, concurrent, parallel pattern fault simulation. Sampling, and statistical fault analysis. (Chapter 5)

Test Generation:

Combinational logic - basic principles and basic methods, D-algorithm, and PODEM algorithms. ATPG system issues and solution. (Chapter 7)

Testability Measures:

Purpose, origin, and SCOAP measure and its applications. (Chapter 6)

Sequential Circuit Test Generation:

Time frame expansion approach. FASTEST approach. Use of 9-value logic, forward, reverse and hybrid test generators. Simulation based approaches. Sequential ATPG systems. (Chapter 8 and paper # 2)

Functional Testing:

Checking experiment approach for sequential circuits.
Structure dependent and independent testing of combinational and sequential circuits (including exhaustive, pseudo-exhaustive and sensitized partitioned testing of combinational circuits).
Functional testing of microprocessors.
(Papers # 3, lectures, and handouts given during class)

Memory Testing:

Testing and test algorithms for memories with a focus on fault models, march tests, and NPSF test algorithms. (Chapter 9)

Current Testing:

Principles of I_{DDQ} testing, its applications and its future. (Chapter 13)

DFT:

Ad hoc and structured techniques for DFT. Full scan and Partial scan. Scan overhead and test time issue. Acyclic circuits. Scan variations. (Chapter 14)

BIST:

BIST economics. Logic BIST: exhaustive, pseudoexhaustive, random and LFSR based.

LFSR: theory, TPG, RC.

BIST architectures: BILBO, test/clock and test/scan. Aliasing issue (concept level) and other limitations. (Chapter 15 and notes on LFSR)

Boundary Scan:

Motivation, standard and its working. (Chapter 16)

Note:

I will pretty much be around during the final week if you have any questions. However, I will observe the following additional office hours before the exam so that you can simply drop in:

December 16 – Friday – 2:30 PM to 4:00 PM

December 17 – Saturday – before the exam 10:00 AM - 12:00 Noon

If you may have questions and you see me in office, I will be glad to see you.