

**Department of Electrical and Computer Engineering
University of Wisconsin–Madison**

**ECE 553: Testing and Testable Design of Digital Systems
Fall 2009-2010**

TENTATIVE COURSE OUTLINE

WEEK START	# OF LECT.	TOPIC(S)	SOURCE(S)
Aug. 31	1	Introduction, Test process	Ch. 1
Sept. 7	2	Test equipment, Test Economics, Logic Modeling	paper, Ch. 2, 3, 4
Sept. 14	2	Logic and Fault Simulation	Ch. 5
Sept. 21	2	Testing basics, Combinational test generation, ATPG Algorithms: D-Algorithm, PO-DEM, FAN	Ch. 7
Sept. 28	2	Combinational test generation (contd.)	Ch. 7
Oct. 5	2	Testability Measure, ATPG systems	Ch. 7, 6
Oct. 12	2	Sequential Circuit ATPG	Ch. 8 and paper
Oct. 19	2	ATPG (contd.), Functional Testing: Checking Experiments	paper

WEEK START	# OF LECT.	TOPIC(S)	SOURCE(S)
Oct. 26	2	Functional Testing: Checking Experiments (contd.), structure based, organization/architecture based (Microprocessor) testing	Ref, Ch. 9
Nov. 2	2	I may be away at ITC on Nov. 2-5 Preparation for midterm Buffer/Review before Examination	
Nov. 9		Midterm Exam - Nov. 9, Monday Evening Room TBA Engineering Hall	
Nov. 9	2	Memory testing, IDDQ Testing	Ch. 9, 13
Nov. 16	2	Design for Testability	Ch. 14
Nov. 23	1	Design for Testability (contd.) <i>I may be at ATS Nov 24-26</i> (Thanksgiving week)	
Nov. 30	2	Built-In Self-Test	Ch 15
Dec. 7	2	Boundary Scan, System Test, Research Directions, Novel and New Concepts Buffer/Review	Ch. 16, 18
Dec. 14	1	Mixed Signal Testing, Research Directions, Novel and New Concepts Buffer/Review	
Dec. 17	Thursday	Final Examination as per timetable at 10:05 AM	