

**Department of Electrical and Computer Engineering
University of Wisconsin–Madison**

**ECE 553: Testing and Testable Design of Digital Systems
Fall 2011-2012**

TENTATIVE COURSE OUTLINE

WEEK START	# OF LECT.	TOPIC(S)	SOURCE(S)
Sept. 5	2	Introduction, Test process and test equipment, Test Economics	Ch1, paper, Ch. 2, 3
Sept. 12	2	Logic Modeling, Fault Modeling	Ch. 4
Sept. 19	2	Logic and Fault Simulation Combinational test generation basics I may be away at ITC on Sept. 18-23	Ch. 5 Ch. 7
Sept. 26	2	Combinational test generation (contd.) ATPG Algorithms: D-Algorithm, PODEM, FAN	Ch. 7
Oct. 3	2	Test Generation (contd.) Testability Measure, ATPG systems	Ch. 7 Ch. 6
Oct. 10	2	Sequential Circuit ATPG	Ch. 8 and paper
Oct. 17	2	ATPG (contd.), Functional Testing: Checking Experiments	paper
Oct. 24	2	Functional Testing: Checking Experiments (contd.), structure based, organization/architecture based (Microprocessor) testing	Ref, Ch. 9
Oct. 31	2	Memory testing, IDDQ Testing	Ch. 9, 13

WEEK START	# OF LECT.	TOPIC(S)	SOURCE(S)
Nov. 7		Design for Testability Buffer/Review before Examination Midterm Exam - Nov. 10, Thursday Evening Room 1153 ME Time: 7:15 – 8:45 PM	Ch. 14
Nov. 14	2	Design for Testability (contd.)	Ch. 14
Nov. 21		No lecture <i>I will be at ATS Nov 18-28</i> (Thanksgiving week)	
Nov. 28	2	Built-In Self-Test <i>VLSI design website should be active</i>	Ch 15
Dec. 5	2	Built-In Self-Test (Contd.) Boundary Scan, System Test	Ch 15 Ch. 16, 18
Dec. 12	2	Mixed Signal Testing, Research Directions, Novel and New Concepts Buffer/Review	
Dec. 17	Saturday	Final Examination as per timetable at 2:45 PM	