

**Department of Electrical and Computer Engineering
University of Wisconsin–Madison**

**ECE 553: Testing and Testable Design of Digital Systems
Fall 2011-2012**

READING LIST

The last two papers deals with a couple of important research issues

- [1] T. W. Williams and N. C. Brown, “Defect level as a function of fault coverage,” *IEEE Transactions on Computers*, vol. C-30, pp. 987–988, Dec. 1981.
- [2] T. P. Kelsey, K. K. Saluja, and S. Y. Lee, “An efficient algorithm for sequential circuit test generation,” *IEEE Transactions on Computers*, vol. C-43, pp. 1361–1371, Nov. 1993.
- [3] F. C. Hennie, “Fault detecting experiments for sequential circuits,” in *Proc. 5th Annual Symposium on Switching and Automata Theory*, pp. 95–110, 1964.
- [4] K. K. Saluja, “Linear feedback shift register: Theory and applications.” Lecture notes, Apr. 1991.
- [5] K. K. Saluja and C. R. Kime, “Automatic test pattern generation (ATPG) tool set.” Department of Electrical and Computer Engineering, University of Wisconsin - Madison, Aug. 1995, Revised 2004.
- [6] C. Yao, K. K. Saluja, and P. Ramanathan, “Power and thermal constrained test scheduling under deep submicron technologies,” *IEEE Transactions on Computer-Aided Design*, vol. 30, pp. 317–322, Feb. 2011.
- [7] N. A. Toubas, “Survey of test vector compression techniques,” *IEEE Design & Test of Computers*, vol. 23, pp. 294–303, July-August 2006.