ECE 553: TESTING AND TESTABLE DESIGN OF DIGITAL SYSTES

Motivation and Introduction

Overview

- Motivation
- About the Course and the Instructor
  - Conduct
  - Outline
  - Coursepack
- Introduction
  - VLSI realization process
  - Contract between design house and fab vendor
  - Test v/s verification
  - Need for testing: doing business, ideal v/s real testing
  - Levels of testing – rule of 10 (or 20)
  - Cost of manufacturing

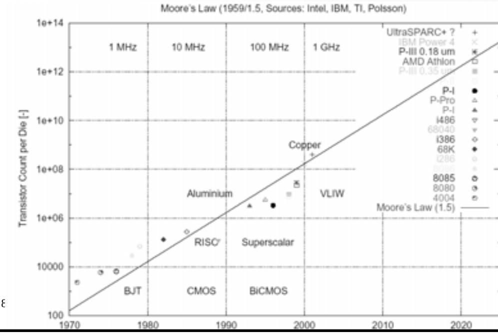
Motivation

- Where do the manufacturing $ go?
- Overhead of one or two photomicrographs
  - What is test on a chip?
- Course conduct
  - Your responsibilities and mine
- Course outline
- Course material information
  - References and reading material

Motivation: Moore's Law

Complexity Growth of VLSI circuits

Source (Copp, *Int. AOC EW Conf., 2002*)



Thermal Effect of Moore's law

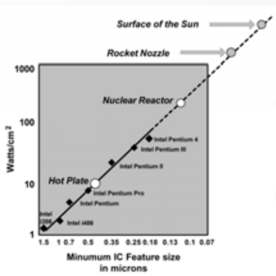
❖ Moore's law

Greater packaging densities

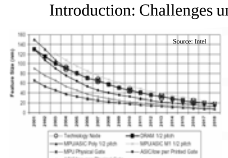
Higher power densities

Higher temperature

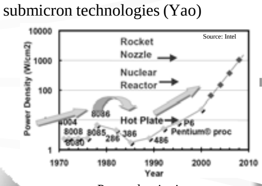
❖ Effects
- ❖ Reliability
- ❖ Performance
- ❖ Power
- ❖ Cooling cost



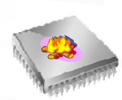
Introduction: Challenges under deep submicron technologies (Yao)

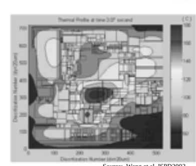


Chip size decreases

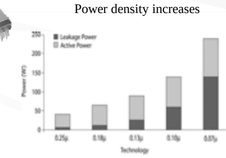


Power density increases





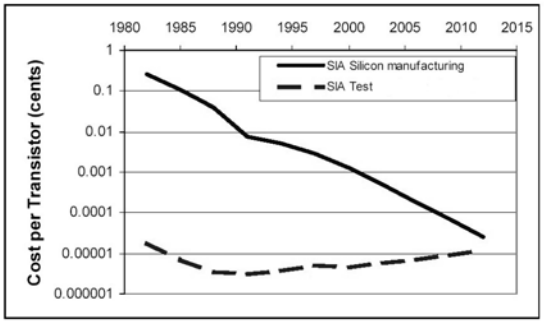
Chip becomes hotter



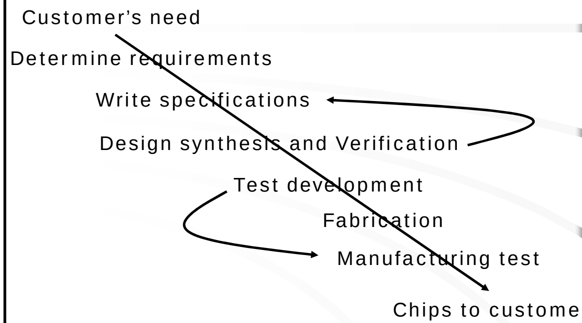
Leakage power make it worse

Microprocessor Cost per Transistor

Cost of testing will *EXCEED* cost of design/manufacturing
(Source: ITR-Semiconductor, 2002)



VLSI Realization Process



Present and Future*

	1997 -2001	2003 - 2010
Feature size (micron)	0.25 - 0.15	0.13 - 0.045
Transistors/sq. cm	4 - 10M	18 - 90M
Pin count	100 - 900	160 - 1675
Clock rate (MHz)	200 - 730	530 - 4000
Power (Watts)	1.2 - 61	2 - 96

* SIA Roadmap

Contract between a design house and a fab vendor

- Design is complete and checked (verified)
- Fab vendor: How will you test it?
- Design house: I have checked it and …
- Fab vendor: But, how would you test it?
- Desing house: Why is that important? It is between I and my clients – it is none of your business
- Fab vendor – Sorry you can take your business some where else.

complete the story and determine the reasons for the importance of test generation etc.

Contract between design …

Hence:

- "Test" must be comprehensive
- It must not be "too long"

Issues:

- Model possible defects in the process
  - Understand the process
- Develop logic simulator and fault simulator
- Develop test generator
- Methods to quantify the test efficiency

Verification v/s Testing

Definitions

- Design synthesis: Given an I/O function, develop a procedure to manufacture a device using known materials and processes.
- Verification: Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.
- Test: A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.

Verification v/s Testing

- Verifies correctness of design.
- Performed by simulation, hardware emulation, or formal methods.
- Performed once prior to manufacturing.
- Responsible for quality of design.

- Verifies correctness of manufactured hardware.
- Two-part process:
  - 1. Test generation: software process executed once during design
  - 2. Test application: electrical tests applied to hardware
- Test application performed on every manufactured device.
- Responsible for quality of devices.

Need for testing

- Functionality issue
  - Does the circuit (large or small) work?
- Density issue
  - Higher density ⇒ higher failure probability
- Application issue
  - Life critical applications
- Maintenance issue
  - Need to identify failed components
- Cost of doing business
- What does testing achieve?
  - Discard only the "bad product"? – see next three slides

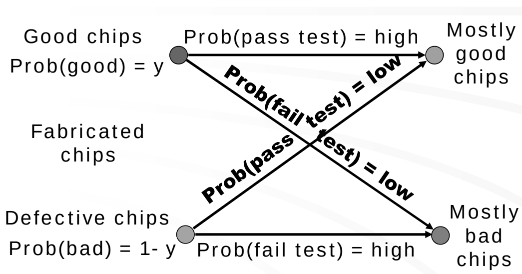
Problems of Ideal Tests

- Ideal tests detect all defects produced in the manufacturing process.
- Ideal tests pass all functionally good devices.
- Very large numbers and varieties of possible defects need to be tested.
- Difficult to generate tests for some real defects. *Defect-oriented testing is an open problem.*

Real Tests

- Based on analyzable fault models, which may not map on real defects.
- Incomplete coverage of modeled faults due to high complexity.
- Some good chips are rejected. The fraction (or percentage) of such chips is called the *yield loss.*
- Some bad chips pass tests. The fraction (or percentage) of bad chips among all passing chips is called the *defect level.*

Testing as Filter Process



Levels of testing (1)

- Levels
  - Chip
  - Board
  - System
    - Boards put together
    - System-on-Chip (SoC)
  - System in field
- Cost – Rule of 10
  - It costs 10 times more to test a device as we move to higher level in the product manufacturing process

Levels of testing (2)

- Other ways to define levels – these are important to develop correct “fault models” and “simulation models”
  - Transistor
  - Gate
  - RTL
  - Functional
  - Behavioral
  - Architecture
- Focus: Chip level testing – gate level design

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Cost of Testing

- *Design for testability* (DFT)
  - Chip area overhead and yield reduction
  - Performance overhead
- Software processes of test
  - Test generation and fault simulation
  - Test programming and debugging
- Manufacturing test
  - *Automatic test equipment* (ATE) capital cost
  - Test center operational cost

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Cost of Manufacturing Testing in 2000AD

- 0.5-1.0GHz, analog instruments,1024 digital pins: ATE purchase price
  - = $1.2M + 1,024 x $3,000 = $4.272M
- Running cost (five-year linear depreciation)
  - = Depreciation + Maintenance + Operation
  - = $0.854M + $0.085M + $0.5M
  - = $1.439M/year
- Test cost (24 hour ATE operation)
  - = $1.439M/(365 x 24 x 3,600)
  - = 4.5 cents/second

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Roles of Testing

- Detection: Determination whether or not the *device under test* (DUT) has some fault.
- Diagnosis: Identification of a specific fault that is present on DUT.
- Device characterization: Determination and correction of errors in design and/or test procedure.
- *Failure mode analysis* (FMA): Determination of manufacturing process errors that may have caused defects on the DUT.

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Summary

- About the course
- Expectations
- Why test?
- Cost issue – First look

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