Motivation

- Early 1990's – Fabrication Line had 50 to 1000 defects per million (dpm) chips
  - IBM wants to get 3.4 defects per million (dpm) chips (0 defects, $6\sigma$)
- Conventional way to reduce defects:
  - Increasing test fault coverage
  - Increasing burn-in coverage
  - Increase Electro-Static Damage awareness
- Newer way to reduce defects:
  - $I_{DDQ}$ Testing – also useful for Failure Effect Analysis

Stuck-at Faults Detected by $I_{DDQ}$ Tests

- Bridging faults with stuck-at fault behavior
  - Levi – Bridging of a logic node to $V_{DD}$ or $V_{SS}$ – few of these
  - Transistor gate oxide short of 1 KΩ to 5 KΩ
- Floating MOSFET gate defects – do not fully turn off transistor
NAND Open Circuit Defect – Floating gate

- The fault manifests as stuck-at, weak ON for N-FET, or delay fault
- Some manifestations can be tested by IDDQ tests

Floating Gate Defects

- Small break in logic gate inputs (100 – 200 Angstroms) lets wires couple by electron tunneling
  - Delay fault and $I_{DDQ}$ fault
- Large open results in stuck-at fault – not detectable by $I_{DDQ}$ test

Bridging Faults S1 – S5

- Caused by absolute short (< 50 Ω) or higher $R$
- Segura et al. evaluated testing of bridges with 3 CMOS inverter chain
- $I_{DDQRb}$ tests fault when $R_b > 50$ KΩ or $0 \leq R_b \leq 100$ KΩ
- Largest deviation when $V_{in} = 5$ V bridged nodes at opposite logic values

$SI I_{DDQ}$ Depends on $K, Rb$

- $K$ is ratio of width of $n_2$ v/s $n_1$
- $I_{DDQ}$ ($\mu$A)

Delay Faults

- Most random CMOS defects cause a timing delay fault, not catastrophic failure
- Many delay faults detected by $I_{DDQ}$ test – late switching of logic gates keeps $I_{DDQ}$ elevated
- Delay faults not detected by $I_{DDQ}$ test
  - Resistive fault in interconnect
  - Increased transistor threshold voltage fault

Leakage Faults

- Gate oxide shorts cause leaks between gate & source or gate & drain

Weak Faults

- $nFET$ passes logic 1 as 5 V – $V_{Th}$
- $pFET$ passes logic 0 as 0 V + $|V_{Th}|$
- Weak fault – one device in C-switch does not turn on
  - Causes logic value degradation in C-switch
Transistor Stuck-Closed Faults

- Due to gate oxide short (GOS)
- \( k \) = distance of short from drain
- \( R_s \) = short resistance
- \( I_{DDQ} \) current results show 3 or 4 orders of magnitude elevation

Gate Oxide Short

Logic / \( I_{DDQ} \) Testing Zones

Fault Coverages for \( I_{DDQ} \) Fault Models

Instrumentation Problems

- Need to measure < 1 \( \mu \)A current at clock > 10 kHz
- Off-chip \( I_{DDQ} \) measurements degraded
  - Pulse width of CMOS IC transient current
  - Impedance loading of tester probe
  - Current leakages in tester
  - High noise of tester load board
- Much slower rate of current measurement than voltage measurement

Sematech Study

- IBM Graphics controller chip – CMOS ASIC, 166,000 standard cells
- 0.8 \( \mu \)m static CMOS, 0.45 \( \mu \)m Lines (\( L_{eff} \)), 40 to 50 MHz Clock, 3 metal layers, 2 clocks
- Full boundary scan on chip
- Tests:
  - Scan flush – 25 ns latch-to-latch delay test
  - 99.7% scan-based stuck-at faults (slow 400 ns rate)
  - 52% SAF coverage functional tests (manually created)
  - 90% transition delay fault coverage tests
  - 96% pseudo-stuck-at fault cov. \( I_{DDQ} \) Tests
Sematech Results

- Test process: Wafer Test → Package Test
  → Burn-In & Retest → Characterize & Failure Analysis
- Data for devices failing some, but not all, tests.
  \[ I_{DDQ} (5 \mu A \text{ limit}) \]

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Sematech Conclusions

- Hard to find point differentiating good and bad devices for \( I_{DDQ} \) & delay tests
- High # passed functional test, failed all others
- High # passed all tests, failed \( I_{DDQ} > 5 \mu A \)
- Large # passed stuck-at and functional tests
  - Failed delay & \( I_{DDQ} \) tests
- Large # failed stuck-at & delay tests
  - Passed \( I_{DDQ} \) & functional tests
- Delay test caught delays in chips at higher Temperature burn-in – chips passed at lower T.

Limitations of \( I_{DDQ} \) Testing

- Sub-micron technologies have increased leakage currents
  - Transistor sub-threshold conduction
  - Harder to find \( I_{DDQ} \) threshold separating good & bad chips
- \( I_{DDQ} \) tests work:
  - When average defect-induced current greater than average good IC current
  - Small variation in \( I_{DDQ} \) over test sequence & between chips
- Now less likely to obtain two conditions

Summary

- \( I_{DDQ} \) tests improve reliability, find defects causing:
  - Delay, bridging, weak faults
  - Chips damaged by electro-static discharge
- No natural breakpoint for current threshold
  - Get continuous distribution – bimodal would be better
- Conclusion: now need stuck-fault, \( I_{DDQ} \), and delay fault testing combined
- Still uncertain whether \( I_{DDQ} \) tests will remain useful as chip feature sizes shrink further