Overview: Partial-Scan & Scan Variations

- Definition
- Partial-scan architecture
- Scan flip-flop selection methods
- Cyclic and acyclic structures
- Partial-scan by cycle-breaking
- Scan variations
- Scan-hold flip-flop (SHFF)
- Summary

Partial-Scan Definition

- A subset of flip-flops is scanned.
- Objectives:
  - Minimize area overhead and scan sequence length, yet achieve required fault coverage
  - Exclude selected flip-flops from scan:
    - Improve performance
    - Allow limited scan design rule violations
  - Allow automation:
    - In scan flip-flop selection
    - In test generation
  - Shorter scan sequences

Partial-Scan Architecture

Scan Flip-Flop Selection Methods

- Testability measure based
  - Use of SCOAP: limited success.
- Structure based:
  - Cycle breaking
  - Balanced structure
    - Sometimes requires high scan percentage
- ATPG based:
  - Use of combinational and sequential TG

Cycle Breaking

- Difficulties in ATPG
- S-graph and MFVS problem
- Test generation and test statistics
- Partial vs. full scan
- Partial-scan flip-flop
Difficulties in Seq. ATPG

- Poor initializability.
- Poor controllability/observability of state variables.
- Gate count, number of flip-flops, and sequential depth do not explain the problem.
- Cycles are mainly responsible for complexity.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Number of gates</th>
<th>Number of flip-flops</th>
<th>Sequential depth</th>
<th>ATPG CPU s</th>
<th>Fault coverage</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLC</td>
<td>355</td>
<td>21</td>
<td>14*</td>
<td>1.247</td>
<td>89.81%</td>
</tr>
<tr>
<td>Chip A</td>
<td>1,112</td>
<td>39</td>
<td>14</td>
<td>369</td>
<td>98.80%</td>
</tr>
</tbody>
</table>

* Maximum number of flip-flops on a PI to PO path

Benchmark Circuits

<table>
<thead>
<tr>
<th>Circuit</th>
<th>$s_{1196}$</th>
<th>$s_{1238}$</th>
<th>$s_{1488}$</th>
<th>$s_{1494}$</th>
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</thead>
<tbody>
<tr>
<td>PI</td>
<td>14</td>
<td>14</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>PO</td>
<td>14</td>
<td>15</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>FF</td>
<td>18</td>
<td>18</td>
<td>6</td>
<td>6</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Gates</th>
<th>1247</th>
<th>1356</th>
<th>1458</th>
<th>1568</th>
</tr>
</thead>
<tbody>
<tr>
<td>Structure</td>
<td>Cycle-free</td>
<td>Cycle-free</td>
<td>Cyclic</td>
<td>Cyclic</td>
</tr>
<tr>
<td>Sequential depth</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Total faults</td>
<td>3</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Potentially detected faults</td>
<td>0</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Abandoned faults</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Fault efficiency (%)</td>
<td>100.0</td>
<td>100.0</td>
<td>94.8</td>
<td>93.4</td>
</tr>
<tr>
<td>Total test vectors</td>
<td>313</td>
<td>308</td>
<td>525</td>
<td>559</td>
</tr>
</tbody>
</table>

A Partial-Scan Method

- Select a minimal set of flip-flops for scan to eliminate all cycles.
- Alternatively, to keep the overhead low only long cycles may be eliminated.
- In some circuits with a large number of self-loops, all cycles other than self-loops may be eliminated.

Cycle-Free Example

All faults are testable. See Example 8.6.

Relevant Results

- Theorem 8.1: A cycle-free circuit is always initializable. It is also initializable in the presence of any non-flip-flop fault.
- Theorem 8.2: Any non-flip-flop fault in a cycle-free circuit can be detected by at most $d_{seq} + 1$ vectors.
- ATPG complexity: To determine that a fault is untestable in a cyclic circuit, an ATPG program using nine-valued logic may have to analyze $9^{N_{ff}}$ time-frames, where $N_{ff}$ is the number of flip-flops in the circuit.

The MFVS Problem

- For a directed graph find a set of vertices with smallest cardinality such that the deletion of this vertex-set makes the graph acyclic.
- The minimum feedback vertex set (MFVS) problem is NP-complete; practical solutions use heuristics.
- A secondary objective of minimizing the depth of an acyclic graph is useful.
Test Generation

- Scan and non-scan flip-flops are controlled from separate clock PIs:
  - Normal mode: Both clocks active
  - Scan mode: Only scan clock active
- Seq. ATPG model:
  - Scan flip-flops replaced by PI and PO
  - Seq. ATPG program used for test generation
  - Scan register test sequence, 001100..., of length $n_{sff} + 4$ applied in the scan mode
  - Each ATPG vector is preceded by a scan-in sequence to set scan flip-flop states
  - A scan-out sequence is added at the end of each vector sequence
- Test length = $(n_{ATPG} + 2) n_{sff} + n_{ATPG} + 4$ clocks

Partial Scan Example

- Circuit: TLC
- 355 gates
- 21 flip-flops

<table>
<thead>
<tr>
<th>Scan flip-flops</th>
<th>Max. cycle length</th>
<th>Depth*</th>
<th>Fault cov.</th>
<th>ATPG vectors</th>
<th>Test seq. length</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>4</td>
<td>14</td>
<td>99.01%</td>
<td>805</td>
<td>805</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>10</td>
<td>95.90%</td>
<td>247</td>
<td>1,249</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>5</td>
<td>99.20%</td>
<td>136</td>
<td>1,382</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>3</td>
<td>100.00%</td>
<td>112</td>
<td>1,256</td>
</tr>
<tr>
<td>21</td>
<td>0</td>
<td>0</td>
<td>100.00%</td>
<td>52</td>
<td>1,190</td>
</tr>
</tbody>
</table>

* Cyclic paths ignored

Partial vs. Full Scan: S5378

<table>
<thead>
<tr>
<th></th>
<th>Number of combinational gates</th>
<th>Number of non-scan flip-flops</th>
<th>Number of scan flip-flops</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2,781</td>
<td>179</td>
<td>0</td>
</tr>
<tr>
<td>(10 gates each)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>30</td>
<td>179</td>
</tr>
<tr>
<td>(14 gates each)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.0%</td>
<td>2.63%</td>
<td>15.68%</td>
</tr>
<tr>
<td></td>
<td>4,603</td>
<td>4,603</td>
<td>4,603</td>
</tr>
<tr>
<td></td>
<td>3540</td>
<td>6579</td>
<td>214,028</td>
</tr>
<tr>
<td></td>
<td>70.0%</td>
<td>93.7%</td>
<td>99.1%</td>
</tr>
<tr>
<td></td>
<td>70.9%</td>
<td>99.5%</td>
<td>100.0%</td>
</tr>
<tr>
<td></td>
<td>414</td>
<td>1,117</td>
<td>585</td>
</tr>
<tr>
<td>Number of ATPG vectors</td>
<td>414</td>
<td>34,691</td>
<td>10,662</td>
</tr>
</tbody>
</table>

Scan Variations

- Integrated and Isolated scan methods
  - Scan path: NEC 1968
  - Serial scan: 1973
  - LSSD: IBM 1977
  - Scan set: Univac 1977
  - RAS: Fujitsu/Amdahl 1980

Flip-flop for Partial Scan

- Normal scan flip-flop (SFF) with multiplexer of the LSSD flip-flop is used.
- Scan flip-flops require a separate clock control:
  - Either use a separate clock pin
  - Or use an alternative design for a single clock pin

Scan Set
Scan Set Applications

- **Advantages**
  - Potentially useable in delay testing.
  - Concurrent testing: can sample the system state while the system is running
    - Used in microrollback
- **Disadvantages**
  - Higher overhead due to routing difficulties

Random-Access Scan (RAS)

- Logic test: reduced test length.
- Delay test: Easy to generate single-input-change (SIC) delay tests.
- Advantage: RAS may be suitable for certain architecture, e.g., where memory is implemented as a RAM block.
- Disadvantages:
  - Not suitable for random logic architecture
  - High overhead – gates added to SFF, address decoder, address register, extra pins and routing – BUT these are addressed by Dong Baik in his Ph.D. work (ITC 2005).

RAS Flip-Flop (RAM Cell)

- Applications:
  - Reduce power dissipation during scan
  - Isolate asynchronous parts during scan test
  - Delay testing

Scan-Hold Flip-Flop (SHFF)

- The control input HOLD keeps the output steady at previous state of flip-flop.

RAS Applications
Summary

- Partial-scan is a generalized scan method; scan can vary from 0 to 100%.
- Elimination of long cycles can improve testability via sequential ATPG.
- Elimination of all cycles and self-loops allows combinational ATPG.
- Partial-scan has lower overheads (area and delay) and reduced test length.
- Partial-scan allows limited violations of scan design rules, e.g., a flip-flop on a critical path may not be scanned.