

## ECE 553: TESTING AND TESTABLE DESIGN OF DIGITAL SYSTEMS

Test Economics:  
Cost analysis and model fitting

### Benefits and Costs of DFT

| Level  | Design and test | Fabrication | Manuf. Test | Maintenance test | Diagnosis and repair | Service interruption |
|--------|-----------------|-------------|-------------|------------------|----------------------|----------------------|
| Chips  | + / -           | +           | -           |                  |                      |                      |
| Boards | + / -           | +           | -           |                  | -                    |                      |
| System | + / -           | +           | -           | -                | -                    | -                    |

+ Cost increase  
 - Cost saving  
 +/- Cost increase may balance cost reduction

9/3/2009 2

### VLSI Defects

Unclustered defects  
 Wafer yield =  $12/22 = 0.55$

Clustered defects (VLSI)  
 Wafer yield =  $17/22 = 0.77$

9/3/2009 3

### Test Coverage from Fault Simulator

9/3/2009 4

### Measured Chip Fallout

9/3/2009 5

### Model Fitting

$Y(1) = 0.7623$   
 $Y(T)$  for  $A=2.1$  and  $\beta = 0.083$

9/3/2009 6

