

ECE 553: TESTING AND TESTABLE DESIGN OF DIGITAL SYSTEMS

Logic Modeling

Overview

- Motivation
- Logic Modeling
 - Model types
 - Models at different levels of abstractions
 - Models and definitions
- Summary

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Motivation

- Models are often easier to work with
- Models are portable
- Models can be used for simulation, thus avoiding expensive hardware/actual circuit implementation
- Nearly all engineering systems are studied using models
- All the above apply for logic as well as for fault modeling

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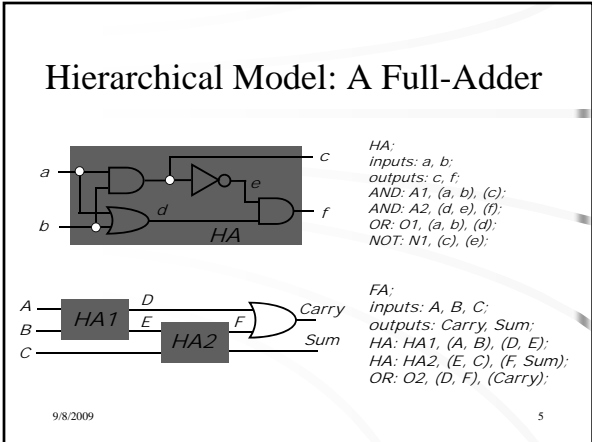
Logic Modeling – Model types

- Behavior
 - System at I/O level
 - Timing inf provided
 - Internal details missing
- Functional
 - DC behavior – no timing
- Structural
 - Gate level description

- External representation
- Internal representation

- Models are often described using an hierarchy

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Modeling Levels

| Modeling level | Circuit description | Signal values | Timing | Application |
|------------------------|---|-------------------------|---------------------------------------|--|
| Function behavior, RTL | Programming language-like HDL | 0, 1 | Clock boundary | Architectural and functional verification |
| Logic | Connectivity of Boolean gates, flip-flops and transistors | 0, 1, X and Z | Zero-delay unit-delay, multiple-delay | Logic verification and test |
| Switch | Transistor size and connectivity, node capacitances | 0, 1 and X | Zero-delay | Logic verification |
| Timing | Transistor technology data, connectivity, node capacitances | Analog voltage | Fine-grain timing | Timing verification |
| Circuit | Tech. Data, active/passive component connectivity | Analog voltage, current | Continuous time | Digital timing and analog circuit verification |

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Logic Models and definitions*

- Combinational circuit models
 - Function expressed as truth-table or cubes
 - Cubes and cube intersection can be used during simulation
- Sequential Circuits
 - Structure represented as a collection of flip-flops feeding combinational logic
 - Time frame expansion is possible
- Binary Decision Diagrams (BDD)

* Ref: Abramovici et. Al, *Digital system testing and testable design*

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Logic Models and definitions (2)

- Program model of a circuit
 - Express circuit (gate level) as a program consisting of interconnected logic operations
 - Execute the program to determine circuit output for varying inputs
- RTL model
 - Higher level model of the circuit
- HDL model
 - Examples at this level are verilog HDL and VHDL

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Logic Models and definitions (3)

- Structural model
 - External representation in the form of netlist
 - Examples of this are uw format, iscas format, EDIF, ...
 - Some keywords used in such representation
 - Primary inputs and Primary outputs
 - Gates: AND, OR, NOT, ...
 - Storage: latch, flip-flop
 - Connections: lines, nets
 - Fanin: number of inputs to a gate
 - Fanout: number of lines a signal feeds
 - Fanoutfree circuit: every line or gate has a fanout of one

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Netlist Format: Two Examples

| UW format | ISCAS format |
|---------------------|-----------------------|
| # gate connected to | output = gate(inputs) |
| 1 PI 4, 5 ; | INPUT(G1) |
| 2 PI 3, 6 ; | INPUT(G2) |
| 3 not 5 ; | OUTPUT(G7) |
| 4 not 6 ; | G3 = NOT(G2) |
| 5 and 7 ; | G4 = NOT(G1) |
| 6 and 7 ; | G5 = AND(G1, G3) |
| 7 or 8 ; | G6 = AND(G2, G4) |
| 8 PO ; | G7 = OR(G5, G6) |

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Logic Models and definitions (4)

- Structural model
 - Internal representation in the form of tables
 - Tables of gates and storage elements (names)
 - Tables of connections
 - Tables of fanin and fanouts
 - Objective is to make the storage and search processes (integral part of simulation) more efficient
 - Knowledge of data structures and algorithms is very useful

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Logic Models and definitions (5)

- Additional useful terms
 - Graph representation
 - Reconvergent fanouts
 - Stems and branches
 - Logic levels in a circuit
 - “levelization” of a circuit

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Summary

- Modeling of logic circuit offers many advantages
- Many modeling levels exist and are used
- Gate level models are most prevalent in logic testing

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