

# ECE 553: TESTING AND TESTABLE DESIGN OF DIGITAL SYSTEMS

## Fault Modeling

## Overview

- Motivation
- Fault Modeling
  - Why model faults?
  - Some real defects in VLSI and PCB
  - Common fault models
  - Stuck-at faults
  - Transistor faults
- Summary

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## Motivation

- Models are often easier to work with
- Models are portable
- Models can be used for simulation, thus avoiding expensive hardware/actual circuit implementation
- Nearly all engineering systems are studied using models
- All the above apply for logic as well as for fault modeling

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## Why Model Faults?

- **I/O function tests inadequate for manufacturing (functionality versus component and interconnect testing)**
- **Real defects (often mechanical) too numerous and often not analyzable**
- **A fault model identifies targets for testing**
- **A fault model makes analysis possible**
- **Effectiveness measurable by experiments**

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## Some Real Defects in Chips

- **Processing defects**
  - Missing contact windows
  - Parasitic transistors
  - Oxide breakdown
  - ...
- **Material defects**
  - Bulk defects (cracks, crystal imperfections)
  - Surface impurities (ion migration)
  - ...
- **Time-dependent failures**
  - Dielectric breakdown
  - Electromigration
  - NBII (negative bias temperature instability)
  - ...
- **Packaging failures**
  - Contact degradation
  - Seal leaks
  - ...

Ref.: M. J. Howes and D. V. Morgan, *Reliability and Degradation - Semiconductor Devices and Circuits*, Wiley, 1981.

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## Common Fault Models

- **Single stuck-at faults**
- **Transistor open and short faults**
- **Memory faults**
- **PLA faults (stuck-at, cross-point, bridging)**
- **Functional faults (processors)**
- **Delay faults (transition, path)**
- **Analog faults**
- **For more examples, see Section 4.4 (p. 60-70) of the book.**

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### Fault Dominance

- If all tests of some fault F1 detect another fault F2, then F2 is said to dominate F1.
- Dominance fault collapsing: If fault F2 dominates F1, then F2 is removed from the fault list.
- When dominance fault collapsing is used, it is sufficient to consider only the input faults of Boolean gates. See the next example.
- In a tree circuit (without fanouts) PI faults form a dominance collapsed fault set.
- If two faults dominate each other then they are equivalent.

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### Dominance Example

All tests of F2

Only test of F1

A dominance collapsed fault set

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### Checkpoints

- Primary inputs and fanout branches of a combinational circuit are called *checkpoints*.
- Checkpoint theorem: A test set that detects all single (multiple) stuck-at faults on all checkpoints of a combinational circuit, also detects all single (multiple) stuck-at faults in that circuit.

Total fault sites = 16  
Checkpoints (●) = 10

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### Classes of Stuck-at Faults

- Following classes of single stuck-at faults are identified by fault simulators:
  - *Potentially-detectable fault* -- Test produces an unknown (X) state at *primary output* (PO); detection is probabilistic, usually with 50% probability.
  - *Initialization fault* -- Fault prevents initialization of the faulty circuit; can be detected as a potentially-detectable fault.
  - *Hyperactive fault* -- Fault induces much internal signal activity without reaching PO.
  - *Redundant fault* -- No test exists for the fault.
  - *Untestable fault* -- Test generator is unable to find a test.

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### Multiple Stuck-at Faults

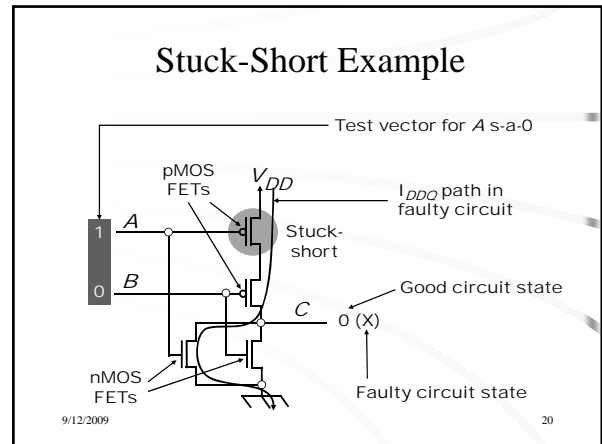
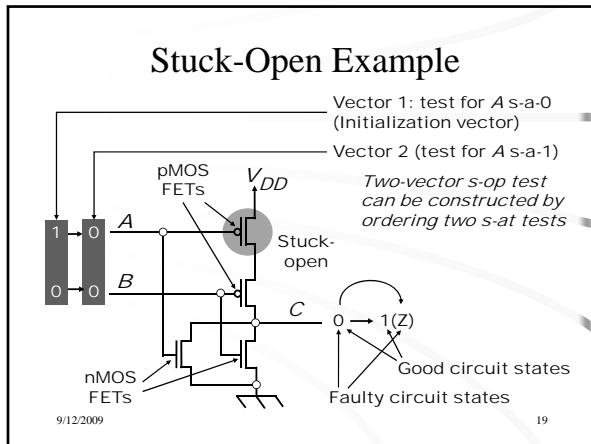
- A multiple stuck-at fault means that any set of lines is stuck-at some combination of (0,1) values.
- The total number of single and multiple stuck-at faults in a circuit with  $k$  single fault sites is  $3^k - 1$ .
- A single fault test can fail to detect the target fault if another fault is also present, however, such masking of one fault by another is rare.
- Statistically, single fault tests cover a very large number of multiple faults.

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### Transistor (Switch) Faults

- MOS transistor is considered an ideal switch and two types of faults are modeled:
  - Stuck-open -- a single transistor is permanently stuck in the open state.
  - Stuck-short -- a single transistor is permanently shorted irrespective of its gate voltage.
- Detection of a stuck-open fault requires two vectors.
- Detection of a stuck-short fault requires the measurement of quiescent current ( $I_{DDQ}$ ).

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- ### Summary
- Fault models are analyzable approximations of defects and are essential for a test methodology.
  - For digital logic single stuck-at fault model offers best advantage of tools and experience.
  - Many other faults (bridging, stuck-open and multiple stuck-at) are largely covered by stuck-at fault tests.
  - Stuck-short and delay faults and technology-dependent faults require special tests.
  - Memory and analog circuits need other specialized fault models and tests.
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