

**Department of Electrical and Computer Engineering  
University of Wisconsin–Madison**

**ECE 553: Testing and Testable Design of Digital Systems  
Fall 2011**

ASSIGNMENT #1

Date: Thursday, September 8, 2011

**Due date: Thursday, September 22, 2011, in class**

1. A certain fabrication process produces 80% good devices. The testing mechanism for the finished ICs has an accuracy of 96%. Find the yield and the defect-level of the ICs. Note: This problem is similar to Problem 1-1 of the text and does not use the yield model of chapter 3.
2. (Bushnell and Agrawal) Problem 1-4  
Note: Use Example 1.2 in the textbook for ATE purchase price, depreciation rate, maintenance, and operating cost
3. (Bushnell and Agrawal) Problem 2-4  
Note: Assume that the setup time is 400ps and the clock-to-Q delay is 450ps. Draw waveform for input/output to explain your test method.
4. (Bushnell and Agrawal) Problem 3-6 but use the following values of  $f, \beta, T$  :  
 $f = 1.4$   
 $\beta = 0.13$   
 $T = 0.94$
5. (Bushnell and Agrawal) Problem 3-7  
Hint: Write the expression  $(1 + (Af/\beta))^{-\beta}$  as an exponential function for  $\beta \rightarrow \infty$ . Of the many ways to do this, one way is to write binomial expansion of the expression and then set  $\beta$  to  $\infty$ .
6. A digital system board uses 64 ICs manufactured in two different independent processes. 48 of the ICs are manufactured in process A with 86% yield and with 96% fault coverage. The remaining ICs (16) are manufactured in process B with 72% yield and with 98% fault coverage. Assuming that the production process and the test program which is used to identify faulty boards are perfect, what is the yield of the manufactured board?  
Note: You will have to choose appropriate yield models to compute the defect levels and specify the yield models that are used.

7. Draw each of the following circuits located at the following locations (These files can be accessed using your CAE-UNIX account).

`~ece553/TESTCAD/nets/hw1-circuits/circuit-1`

`~ece553/TESTCAD/nets/hw1-circuits/circuit-2`

However, you can also access this on the course web page using the links given below this homework link.

Though, I would prefer if you start using CAE-UNIX account now.

8. Using your circuit drawn for *circuit-1* in problem 7, simulate following four vectors and specify the output of each vector.

|    |   |   |   |   |   |
|----|---|---|---|---|---|
| PI | 1 | 2 | 3 | 4 | 5 |
| V1 | 1 | 0 | 0 | 0 | 0 |
| V2 | X | 0 | 0 | 0 | 0 |
| V3 | 0 | 1 | 0 | X | X |
| V4 | 1 | 0 | X | 0 | 1 |