

**Department of Electrical and Computer Engineering
University of Wisconsin–Madison**

**ECE 553: Testing and Testable Design of Digital Systems
Fall 2009**

ASSIGNMENT #1

Date: Thursday, September 10, 2009

Due date: Thursday, September 24, 2009, in class

1. A certain fabrication process produces 75% good devices. The testing mechanism for the finished ICs has an accuracy of 96%. Find the yield and the defect-level of the ICs. Note: This problem is similar to Prob 1-1 from the text and does not use the yield model of chapter 3.
2. (Bushnell and Agrawal) Problem 1-4
Note: Use Example 1.2 in the textbook for ATE purchase price, depreciation rate, maintenance, and operating cost
3. (Bushnell and Agrawal) Problem 2-4
Note: Assume a clock-to-Q delay of 400ps. Draw waveform for input/output to explain devised test method.
4. (Bushnell and Agrawal) Problem 3-6 with changed values of f, β, T as follows :
 $f = 1.51$
 $\beta = 0.13$
 $T = 0.94$
5. (Bushnell and Agrawal) Problem 3-7
Hint: Write the expression $(1 + (Af/\beta))^{-\beta}$ as an exponential function for $\beta \rightarrow \infty$
6. A digital system board uses 64 ICs manufactured in two different independent processes. 48 of the ICs are manufactured in process A with 86% yield and with 96% fault coverage. The remaining ICs (16) are manufactured in process B with 72% yield and with 98% fault coverage. Assuming that the production process and the test program which is used to identify faulty boards are perfect, what is the yield of the manufactured board?
Note: You will have to choose appropriate yield models to compute the defect levels and specify the yield models that are used.
7. Draw each of the following circuits located at the following locations (These files can be accessed using your CAE-UNIX account).

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~ece553/TESTCAD/nets/hw1-circuits/circuit-1
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~ece553/TESTCAD/nets/hw1-circuits/circuit-2
```

8. Using your circuit drawn for *circuit-1* in problem 7, simulate following four vectors and specify the output of each vector.

PI	1	2	3	4	5
V1	0	0	1	0	0
V2	X	0	0	0	0
V3	0	1	0	X	X
V4	1	X	0	0	1