

**Department of Electrical and Computer Engineering
University of Wisconsin–Madison**

**ECE 553: Testing and Testable Design of Digital Systems
Fall 2011**

ASSIGNMENT #1

Date: Thursday, September 8, 2011

Due date: Thursday, September 22, 2011, in class

SOLUTION

1. A certain fabrication process produces 80% good devices. The testing mechanism for the finished ICs has an accuracy of 96%. Find the yield and the defect-level of the ICs. Note: This problem is similar to Problem 1-1 of the text and does not use the yield model of chapter 3.

Use the following convention for this problem:

PQ: chip is good P: chip passes the test
FQ: chip is bad F: chip fails the test

A 80% good device production means, $Prob(PQ) = 0.80$ and $Prob(FQ) = 0.20$. Similarly, from the given data, we can see that $Prob(P/PQ) = 0.96$ and $Prob(P/FQ) = 0.04$. We have to calculate the probability of passing $Prob(P)$ ie. the yield.

$$\begin{aligned} Prob(P) &= Prob(P/PQ) \times Prob(PQ) + Prob(P/FQ) \times Prob(FQ) \\ &= 0.96 \times 0.80 + 0.04 \times 0.20 = 0.776 \end{aligned}$$

$$\begin{aligned} \text{Defect level} &= \frac{\text{Bad chips that pass tests}}{\text{All chips that pass tests}} \\ &= Prob(FQ|P) \\ &= \frac{Prob(P|FQ)Prob(FQ)}{Prob(P)} \\ &= \frac{0.04 \times 0.20}{0.776} = 0.010309 \end{aligned}$$

The defect level is 10,309 ppm (parts per million) and the yield is 77.6%.

2. (Bushnell and Agrawal) Problem 1-4

Note: Use Example 1.2 in the textbook for ATE purchase price, depreciation rate, maintenance, and operating cost

Following Example 1.2 of the book (pp. 10-11), we obtain

$$\text{ATE purchase price} = \$1.2M + 256 \times \$3,000 = \$1.968M$$

Assuming a 20% per year linear rate of depreciation, a maintenance cost of 2% of the price, and an annual operating cost of \$0.5M,

$$\text{Running cost} = \$1.968M \times 0.2 + \$1.968M \times 0.02 + \$0.5M = \$932,960/\text{year}$$

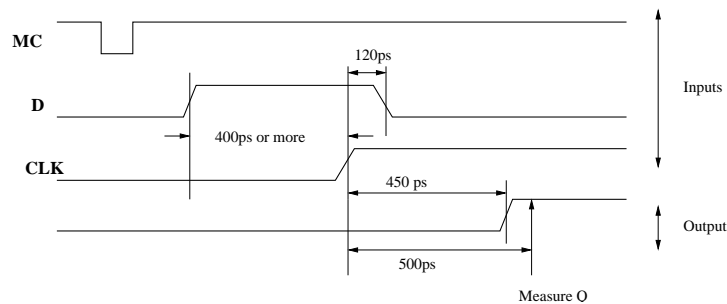
$$\text{Testing cost} = \frac{\$932,960}{365 \times 24 \times 3600} = 2.96 \text{ cents/second}$$

Testing cost of the self-test design is 2.96 cents per second, down from 4.50 cents per second calculated in Example 1.2

3. (Bushnell and Agrawal) Problem 2-4

Note: Assume that the setup time is 400ps and the clock-to-Q delay is 450ps. Draw waveform for input/output to explain your test method.

To test for hold time, $t_{hold} = 120ps$, apply the following waveforms to the chip:



Signal \overline{MC} is used to clear the Q Output. The value on D line is kept stable at logic 1 for at least 400ps before the rising edge of the clock. At an interval of 120ps after the rising CLK edge, we lower the D line. If $Q = 1$ at 500ps after the rising CLK edge, the device passes, otherwise it fails. Using \overline{MS} instead of \overline{MC} , repeat the above waveform sequence, but with D inverted and the expected Q signal also inverted. At an interval of 500ps after the rising CLK edge, again measure Q on the ATE. If $Q = 0$, the device passes, otherwise it fails. The same waveforms are applied simultaneously to all five D lines, and five simultaneous measurements are made on the five Q lines.

4. (Bushnell and Agrawal) Problem 3-6 but use the following values of f, β, T :

$$\begin{aligned} f &= 1.4 \\ \beta &= 0.13 \\ T &= 0.94 \end{aligned}$$

Substituting the given fault density, $f = 1.4 \text{ faults/cm}^2$, the fault clustering parameter, $\beta = 0.13$, and the fault coverage, $T = 0.94$, in Equation 3.20 (page 50 of the book), we obtain the defect level as,

$$\begin{aligned} DL(T) &= 1 - \left(\frac{\beta + T Af}{\beta + Af} \right)^\beta \\ &= 1 - \left(\frac{0.13 + 0.94 \times 1.0 \times 1.4}{0.13 + 1.0 \times 1.4} \right)^{0.13} \\ &= 0.007314 \text{ or } 7314 \text{ parts per million} \end{aligned}$$

The defect level is 7314 parts per million (ppm).

(a) To obtain the fault coverage T for a required defect level of 1,000 ppm, we substitute $DL = 0.001$ in the equation for $DL(T)$ and compute T . Note we will get the expression for T as in problem 3.5.

$$T = \frac{(0.13 + 1.4) \times 0.999^{1/0.13} - 0.13}{1.4} = 0.9916$$

The required fault coverage is 99.16%.

(b) For a defect level of 500 ppm ($DL = 0.0005$), we get

$$T = \frac{(0.13 + 1.4) \times 0.9995^{1/0.13} - 0.13}{1.4} = 0.9958$$

The required fault coverage is 99.58%.

5. (Bushnell and Agrawal) Problem 3-7

Hint: Write the expression $(1 + (Af/\beta))^{-\beta}$ as an exponential function for $\beta \rightarrow \infty$. Of the many ways to do this, one way is to write binomial expansion of the expression and then set β to ∞ .

Defect level, $DL(T)$, given by Equation 3.20 (p. 50 of the book), can be written as:

$$\begin{aligned} DL(T) &= 1 - \frac{(1 + T Af/\beta)^\beta}{(1 + Af/\beta)^\beta} \\ &= 1 - \frac{e^{T Af}}{e^{A f}} = 1 - e^{-A f(1-T)}, \text{ as } \beta \rightarrow \infty \end{aligned}$$

Note that, $\left(1 + \frac{x}{\beta}\right)^{-\beta}$ can be written as e^{-x} as $\beta \rightarrow \infty$ using Taylor expansion. Also, as $\beta \rightarrow \infty$, Equation 3.19 (p. 50 of the book) gives the yield,

$$Y = \left(1 + \frac{Af}{\beta}\right)^{-\beta} = e^{-Af}$$

Substituting this expression for yield in the defect level, we get

$$DL(T) = 1 - (e^{-Af})^{1-T} = 1 - Y^{1-T}$$

which is the required result.

6. A digital system board uses 64 ICs manufactured in two different independent processes. 48 of the ICs are manufactured in process A with 86% yield and with 96% fault coverage. The remaining ICs (16) are manufactured in process B with 72% yield and with 98% fault coverage. Assuming that the production process and the test program which is used to identify faulty boards are perfect, what is the yield of the manufactured board?

Note: You will have to choose appropriate yield models to compute the defect levels and specify the yield models that are used.

The yield model chosen will be $DL = 1 - Y^{1-T}$, because the statistics provided do not specify β and it will be assumed as $\beta \rightarrow \infty$.

For ICs with Process A:

Fault coverage = 96%

Yield = 86%

$$DL1 = (DefectLevel1) = 1 - Y^{(1-T)} = 0.00601475$$

For ICs with Process B:

Fault coverage = 98%

Yield = 72%

$$DL2 = (DefectLevel2) = 1 - Y^{(1-T)} = 0.006548545$$

$$\text{Board Yield} = \text{Pr}(\text{all IC's are fault free}) = (1 - DL1)^{48}(1 - DL2)^{16} = \mathbf{0.6738825}$$

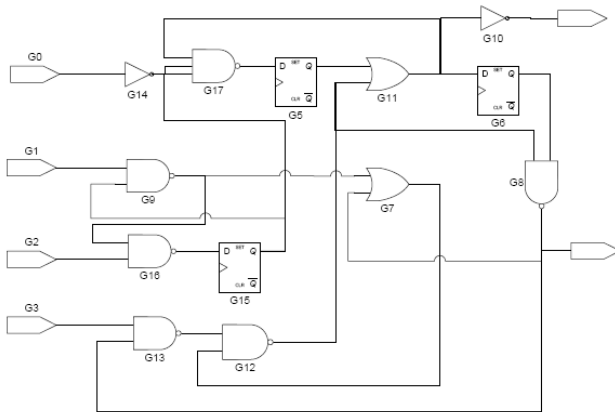
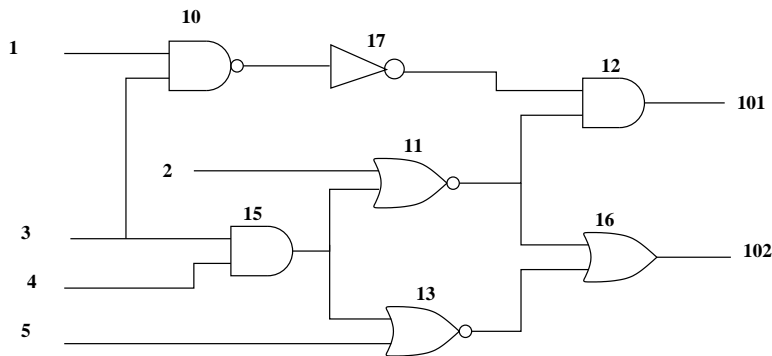
7. Draw each of the following circuits located at the following locations (These files can be accessed using your CAE-UNIX account).

~ece553/TESTCAD/nets/hw1-circuits/circuit-1

~ece553/TESTCAD/nets/hw1-circuits/circuit-2

However, you can also access this on the course web page using the links given below this homework link. Though, I would prefer if you start using CAE-UNIX account now.

See figures next page



8. Using your circuit drawn for *circuit-1* in problem 7, simulate following four vectors and specify the output of each vector.

PI	1	2	3	4	5
V1	1	0	0	0	0
V2	X	0	0	0	0
V3	0	1	0	X	X
V4	1	0	X	0	1

Input and outputs for *circuit-1* are given below:

PI	1	2	3	4	5	P0	101	102
V1	0	0	1	0	0		0	1
V2	X	0	0	0	0		0	1
V3	0	1	0	X	X		0	X
V4	1	X	0	0	1		X	X