Department of Electrical and Computer Engineering
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ECE 553: Testing and Testable Design of Digital Systems
Fall 2009

ASSIGNMENT #2
Date: Friday, September 25, 2009
Due date: Tuesday, October 6, 2009

Solution

1. Compute the total number of stuck-at (single and multiple) faults for a logic in figure. For the circuit of Figure 1, we have

$$\begin{aligned}\text{Number of fault sites} &= \text{PIs} + \text{gates} + \text{fanout branches} \\ &= 16\end{aligned}$$

Therefore,

$$\text{Number of single faults} = 16 \times 2 = 32$$

$$\begin{aligned}\text{Number of single and multiple faults} &= 3^{\text{number of fault sites}} - 1 \\ &= 3^{16} - 1 = 43,046,720\end{aligned}$$

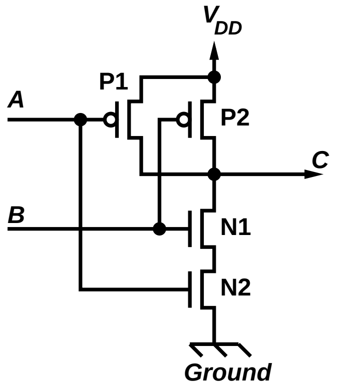
The circuit has 43,046,720 single and multiple stuck-at faults.

$$\begin{aligned}\text{Total number of transitors} &= 2 \times 1 + (2 \times 2 + 2) \times 5 \\ &= 32\end{aligned}$$

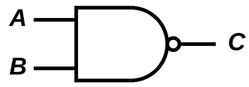
The circuit has 32 stuck-open faults.

2. (Bushnell and Agrawal) Problem 4.5
(a) A two-input NAND gate is shown in the above figure. The following table gives tests for transistor stuck-open (sop) faults:

Test No.	Fault	Test: Vector 1, Vector 2
1	P1 sop	11, 01
2	P2 sop	11, 10
3	N1 sop	01, 11 or 10, 11 or 00, 11
4	N2 sop	01, 11 or 10, 11 or 00, 11



CMOS NAND gate.



Logic NAND gate.

Circuit for Problem 4.5.

Notice that the sop faults of N1 and N2 have exactly the same tests. These two faults are equivalent. Equivalence of transistor faults is discussed in the following paper:

M.-L Flottes, C. Landrault and S. Provossoudovitch, "Fault Modeling and Fault Equivalence in CMOS Technology," *J. Electronic Testing: Theory and Applications*, vol. 2, pp. 229-241, August 1991.

(b) The following sequence of four vectors contains one vector pair for each fault in the above table:

11, 01, 11, 10

Notice that this sequence also detects all single stuck-at faults in the logic model of the NAND gate.

(c) A stuck-at fault in a signal affects two transistors in the two-input NAND gate. For example, the fault A s-a-1 will mean that N1 remains permanently shorted (N1-ssh) and P1 remains permanently open (P1-sop). The following table gives all equivalences:

Stuck-at fault	Equivalent transistor faults
A s-a-1	N2-ssh **and** P1-sop
B s-a-1	N1-ssh **and** P2-sop
C s-a-1	(P1 **or** P2 **or** both ssh) **and** (N1 **or** N2 **or** both sop)
A s-a-0	N2-sop **and** P1-ssh
B s-a-0	N1-sop **and** P2-ssh
C s-a-0	N1-ssh **and** N2-ssh **and** P1-sop **and** P2-sop

Notice that the three equivalent faults, A s-a-0, B s-a-0 and C s-a-0, are actually caused by different faulty transistors. They are detected by the same test (11).

3. given below.

   Faulty functions for the circuit of Figure 4.6 corresponding to the two faults after logical simplification are:

$$m(a\ s-a-0) = b+d$$
$$n(a\ s-a-0) = b \oplus \mathrm{d}$$

(2)

(3)

$$m(c\ s-a-1) = b+d$$
$$n(c\ s-a-1) = b \oplus \mathrm{d}$$

(5)

(6)

   The two faulty functions are indistinguishable and hence **the two faults are equivalent.**

4. For this problem you will use the circuit given in Figure 3.

   (a) The Table 1 gives a fault list for the circuit of Figure 2, after structural fault collapsing. Fill in the blanks with equvalent fault sets for each listed fault. (Validity check: the total number of faults in table should be 38)

   (b) Assume that you are applying exhaustive test set for the circuit in Figure 2. In the Table 2, mark all the faults that are detected by each vector. Note that only the collapsed faults are listed in Table 2. *For this problem you are allowed to use fault simulator (SFSP) of TESTCAD toolset*

   (c) From the cover table of (b),

      i. find minimum number of vectors that detect all detectable faults.
      At least 4 vectors are required to detect all detectable faults.

      ii. list a minimum test set.
      The 4 essential vectors are

$$1100, 1000, 0010, 0001$$

      to detect all detectable faults. There are however a few faults that are undetectable.

Fault	List all equivalent Faults
1/0	3/0, 7/0
1/1	Ø
2/0	Ø
2/1	Ø
3/1	Ø
4/0	Ø
4/1	8/1, 5/1
5/0	Ø
6/0	Ø
7/1	17/0
8/0	Ø
9/0	14/1, 12/0
9/1	Ø
10/0	Ø
10/1	6/1, 11/0
11/1	Ø
12/1	Ø
13/1	Ø
14/0	Ø
15/0	Ø
16/0	19/1 13/0
16/1	Ø
17/1	18/1, 15/1
18/0	Ø
19/0	Ø

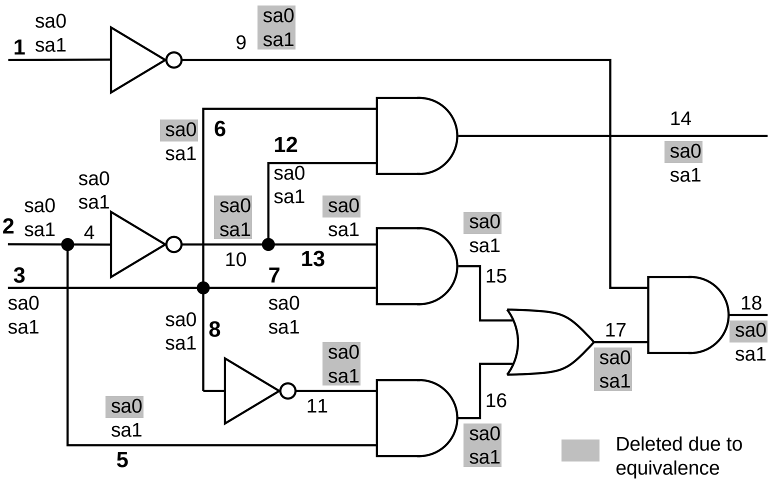
Table 1: Table for problem 4(a)

1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
3	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1/0																
1/1																
2/0					v								v			
2/1	v								v							
4/0					v								v			
4/1	v								v							
5/0			v								v					
6/0		v								v						
7/1																
8/0			v		v		v				v		v		v	
9/0																
9/1	v								v							
10/0													v		v	
10/1	v								v							
11/1		v								v			v	v	v	v
12/1													v	v	v	v
13/1		v	v	v	v	v	v	v	v	v	v	v	v	v	v	v
14/0	v								v				v	v	v	v
15/0													v	v	v	v
16/0	v								v							
16/1																
17/1													v	v	v	v
18/0	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v
19/0		v	v	v	v	v	v	v		v	v	v	v	v	v	v

Table 2: Table for problem 4(b)

5. (Bushnell and Agrawal) Problem 4.11

   (a) The given circuit is shown below with fault sites marked with numbers. The number of potential fault sites is 18.



Circuit for Problem 4.11.

   (b) The figure shows deletion of equivalent faults using an output to input pass. Of the 36 faults, 20 remain, giving a collapse ratio $20/36 = 0.56$.

   (c) Checkpoint lines are shown in boldface numbers. These are three PIs and seven fanout branches. There are ten checkpoints and 20 checkpoint faults. (There are some people treated a single input gate (inverter) as continuation of its input line. Thus, line 2 is assumed to fanout to 5, 12 and 13. There are nine checkpoints and 18 checkpoint faults. For grading, I give full credit for both cases.) Further, s-a-0 faults on lines 6 and 12 are equivalent and any one of them can be chosen. Similarly, s-a-0 faults on 7 and 13 are equivalent, and so are s-a-0 on 5 and s-a-0 on 11. Thus, the set of fault set is reduced to 17, giving a collapse ratio $17/36 = 0.472$.

6. (Bushnell and Agrawal) Problem 4.12. Please use the corrected version of the Definition 4.7 (page 78) in the text for checkpoints in a circuit. The corrected version (also discussed in class) can be found via the link shown for the corrections in the course web page. The correction link URL is

   http://www.ece.wisc.edu/∼va/BOOK/corrections

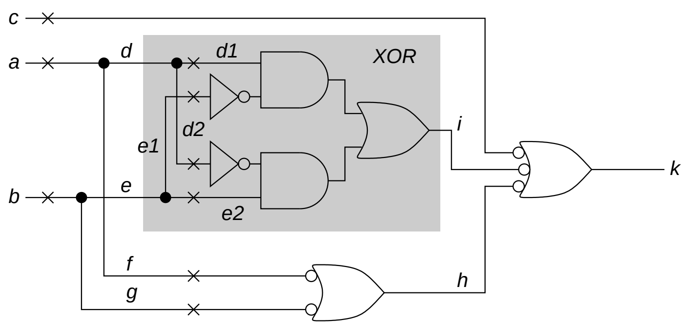
   Once, you see the corrected version of the definition, you will need to know the gate level realization of the Exclusive OR circuit. Use the gate level realization of the Exclusive OR shown in Figure 4.9 of the text. Thus, in the new circuit, with Exclusive OR replaced with its gate equivalent realization, the lines d and e will have fanouts.

Label these fanout signals as d1, d2, e1,e2. The signals d1 and e2 will feed the AND gates and d2 and e1 will be inputs to the NOT gates.

(a) Checkpoints are defined for the signals in a combinational circuit. These signals are the interconnects between Boolean gates, a fact not always explicitly stated. To avoid ambiguity, the definition on page 78 of the book should read as:

Definition 4.7 *Checkpoints. Primary inputs and fanout branches of a combinational circuit consisting only of Boolean gates are called the* checkpoints.

To find checkpoints of the circuit of Figure 4.12, we must replace the exclusive-OR (XOR) function by a primitive Boolean gate implementation. AND, OR, NAND, NOR and NOT are called the *primitive* Boolean gates. Functions such as XOR are sometimes referred to as *complex* gates. In the following figure, we have assumed one such implementation. Our result is, therefore, based on this assumption. Other implementations of the XOR function are possible and can give a different set of checkpoints.

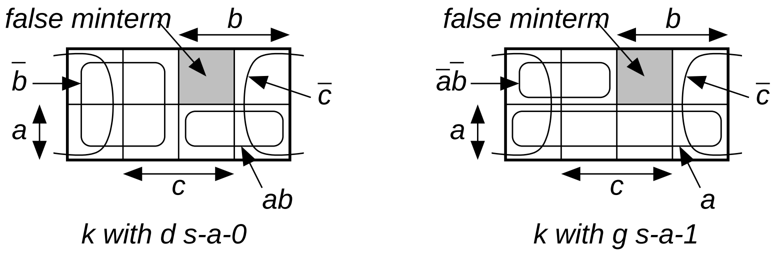


There are eleven checkpoints in this circuit. These include three primary inputs, a, b and c, and eight fanout branches, d, $d1$, $d2$, f, e, $e1$, $e2$ and g. The checkpoint fault set consists of twenty-two faults – s-a-0 and s-a-1 faults on the eleven lines.

(b) We evaluate the output function k corresponding to the two faults:

$$\begin{aligned} k(d\ s-a-0) &= \bar{c} + \bar{b} + \overline{\bar{a} + \bar{b}} \\ &= \bar{c} + \bar{b} + ab \\ k(g\ s-a-1) &= \bar{c} + \overline{a\bar{b} + \bar{a}b} + a \\ &= \bar{c} + \bar{a}\bar{b} + a \end{aligned}$$

The two faulty functions are shown by Karnaugh maps below. In both cases, the functions have exactly one false minterm, $\bar{a}bc$. **Since the two faulty functions are identical the corresponding faults are equivalent**.



Note: this type of fault equivalence is functional and is often difficult to find by typical fault analysis tools, which rely on structurally identifiable equivalences.

7. (Bushnell and Agrawal) Problem 5.26. (Compute the range of fault coverage with 99.7% confidence limit) Assuming that the fault sample size is much smaller than the total fault population, i.e., $N_s \ll N_p$, we use the result of Equation 5.9 (page 124 in the book), which can be written as,

$$\text{Sample size, } N_s = \frac{4.5^2}{\Delta^2} 0.44x(1-x)$$

where $\pm\Delta$ is the 3σ range of the coverage estimate and x is the sample coverage. Using the given data, $\Delta = 0.02$ and $x = 0.70$, we obtain

$$N_s = \frac{4.5^2 \times 0.44 \times 0.7 \times 0.3}{0.02^2} = 4,678 \text{ faults}$$