

Department of Electrical and Computer Engineering
University of Wisconsin–Madison

ECE 553: Testing and Testable Design of Digital Systems
Fall 2009

ASSIGNMENT #3

Date: Tuesday, October 6, 2009

Due date: Thursday, October 22, 2009

1. For the circuit shown in **Fig.1**, perform Parallel pattern single fault simulation targeting the fault h stuck-at-1. You are given 5 vectors to simulate and the vectors are encoded as 11 for 1, 00 for 0 and 01 for X. **State which vectors are able to detect the fault.**

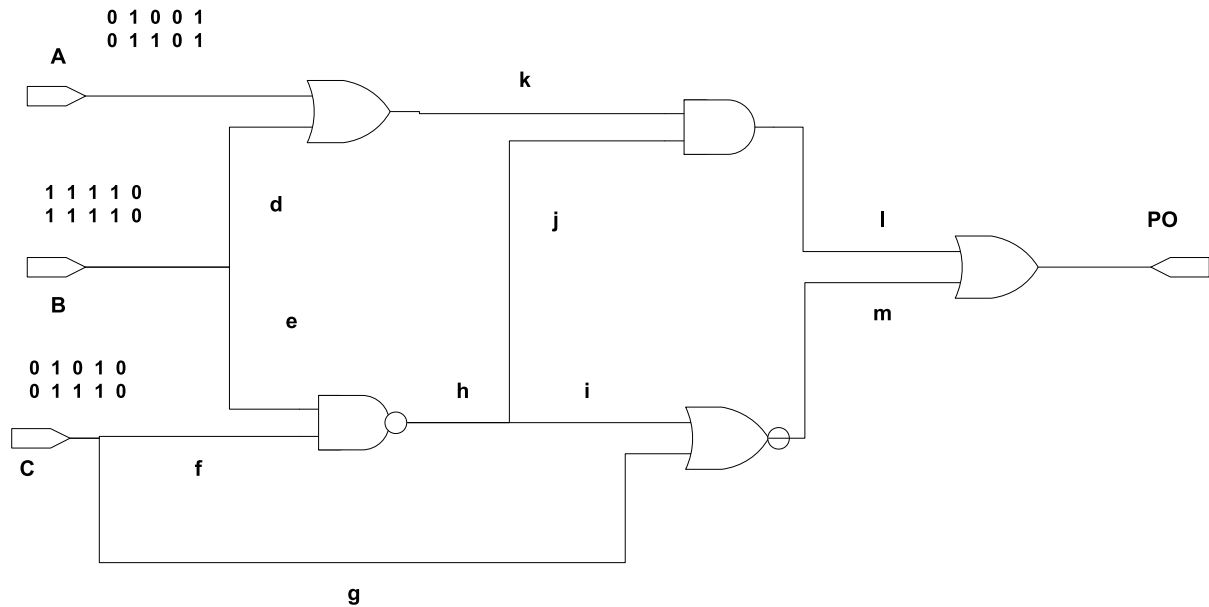


Fig. 1

2. For the **circuit in fig. 2** which is the same circuit as problem 1, perform parallel fault simulation for the **vector** as shown therein with fault-list: k-sa1, h-sa0 and m-sa0. **State which faults are detected by the vector.**

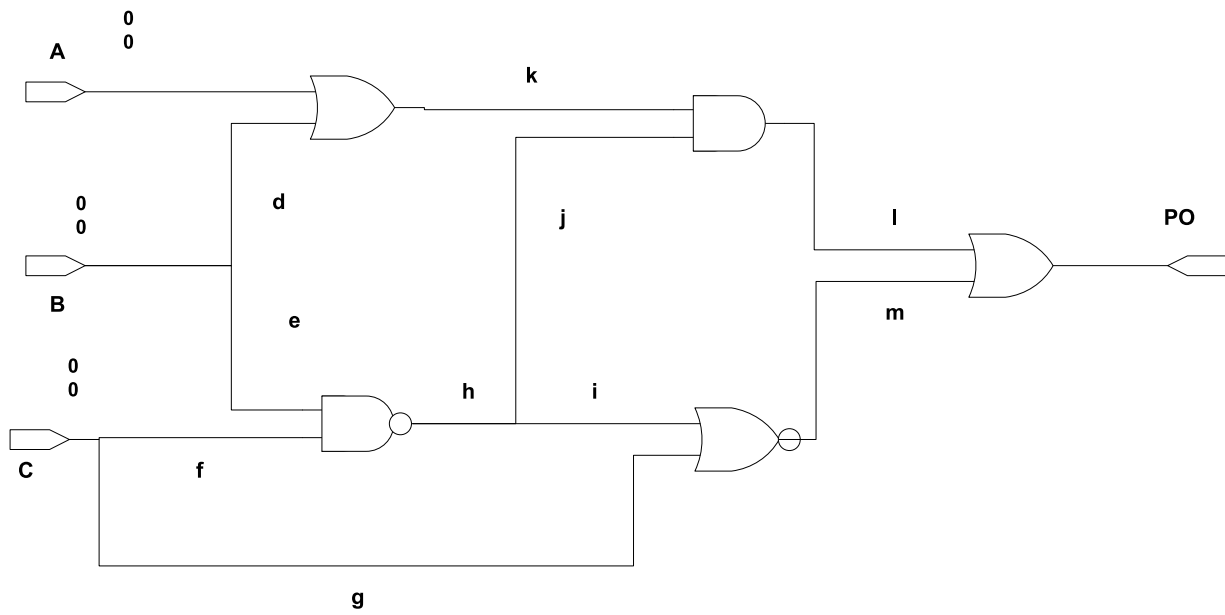


Fig. 2

3. For the circuit in Fig.3, perform deductive fault simulation to determine what faults will be detected at the primary output 'M' for the test vector a=0 b=1 e=1 f=0.

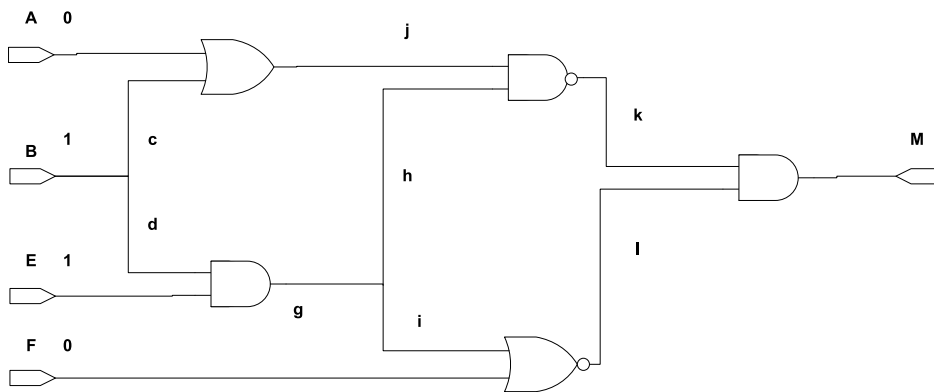


Fig. 3

4. For the circuit in Fig. 4, perform concurrent fault simulation for the following conditions: (i) Initially $ABC=011$. (ii) 1 to 0 “good” event on B.

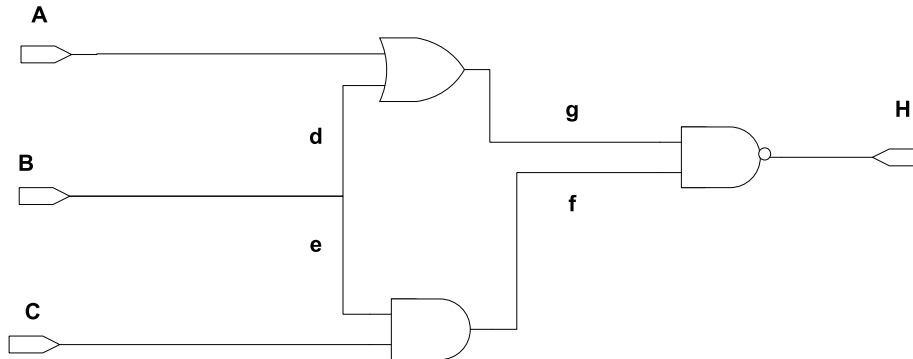


Fig. 4

5. (Bushnell and Agrawal) Problem 7.13

6. (Bushnell and Agrawal) Problem 7.8

Note : While you are performing the PODEM algorithm, follow the rules given below.

- Order: Try to excite the fault first then propagate.
- Backtrace: Follow a path from the objective to a primary input while always following the alphabetical order (e.g. if a gate has input A and B, backtrace on that gate goes to line A first).
- PI assignment: Always assign 0 first, then assign 1 in case of backtrack.
- Choice of D or D_bar : Always try to propagate a D or D_bar from the D-frontier which has the shortest path to the primary output. In the case of tie, follow the alphabetical order.

7. (Bushnell and Agrawal) Problem 6.3

8. (Bushnell and Agrawal) Problem 6.9

9. You are required to work with the circuit n432 and 10 test vectors.

The circuit n432 can be found here:

`/pong/usr0/e/ece553/TESTCAD/nets/hw3-circuits/n432`

The 10 Test Vectors can be found here:

`/pong/usr0/e/ece553/TESTCAD/nets/hw3-circuits/n432.10vec`

Use the testcad tools to answer the following questions.

- a) Apply the given 10 test vectors to n432 and determine the fault coverage. (submit coverage information)
- b) Use PODEM to generate tests for each fault (without intervening fault simulation). Indicate how many tests are generated and which faults are found to be untestable or aborted.
- c) Choose any 10 test vectors from your list of test vectors, then fill in the X's using 'randvec'. Determine the fault coverage of your 10 vectors and compare that with the coverage of 10 vectors obtained in part (a). submit your 10 vectors and the coverage of your vector set.

Note: In all the problems in this homework, if you are asked to compute fault coverage, use the fault list reduced by structural fault equivalence unless mentioned otherwise.