

**Department of Electrical and Computer Engineering
University of Wisconsin–Madison**

**ECE 553: Testing and Testable Design of Digital Systems
Fall 2011**

ASSIGNMENT #3

Solution

- For the circuit shown in the Figure 1, perform Parallel pattern single fault simulation targeting the fault h stuck-at-1. You are given 4 vectors to simulate and the vectors are encoded as 11 for 1, 00 for 0 and 01 for X.

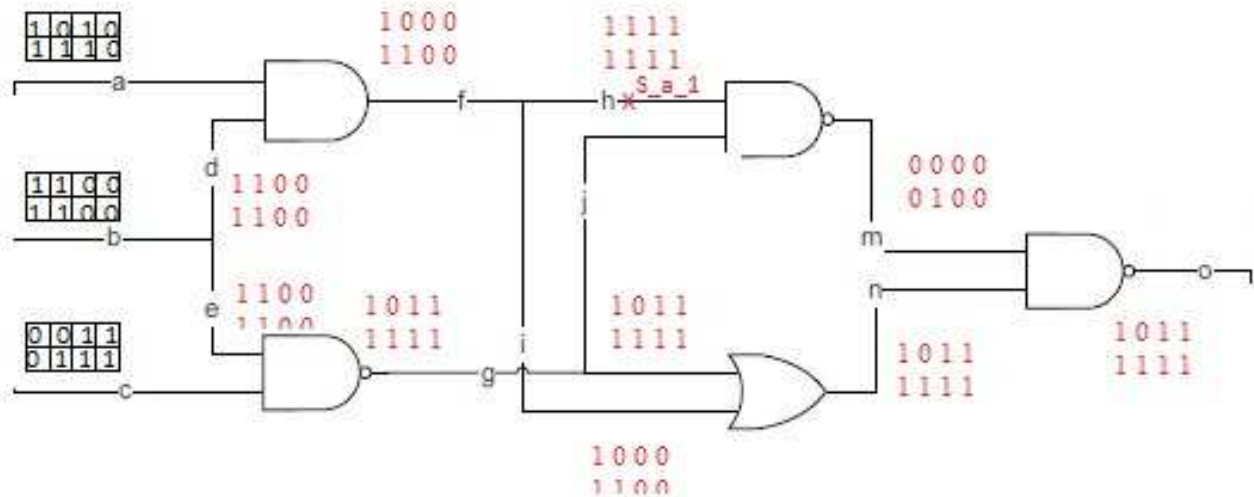


Figure 1: Parallel pattern single fault simulation

From the figure, we can see that vectors 1 and 2 produce a different output from the fault free circuit at the output and hence the fault is detectable under the two vectors. However vector 3 fails to distinguish between the faulty and fault-free circuits at the PO and hence the fault is undetectable under vector 3. Vector 4 is a special case in that it produces an X at the primary output and hence the fault is said to be potentially detectable under vector 4.

2. For the circuit in Figure 2, which is the same circuit as problem 1, perform parallel fault simulation for the vector $abc = 110$ and three faults: d stuck-at-0, h stuck-at-0 and n stuck-at-1 to determine which faults will be detected at the primary output.

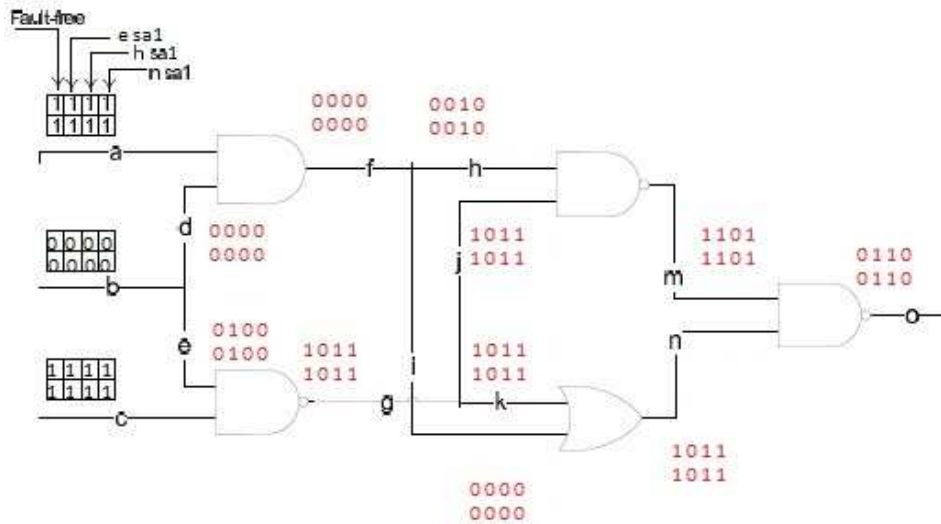


Figure 2: Parallel fault simulation

From the figure, $e\ sa1$ and $h\ sa1$ are detectable by the input, but $nsa1$ is not.

3. For the same circuit shown in figure 1, perform deductive fault simulation to determine what faults will be detected at the primary output h for the test vector $a=1\ b=0\ c=1$.

Solution:

$$\begin{aligned}
 L_a &= \{a/0\} \\
 L_b &= \{b/1\} \\
 L_c &= \{c/0\} \\
 L_d &= \{b/1, d/1\} \\
 L_e &= \{b/1, e/1\} \\
 L_f &= L_d \cap \overline{L_a} \cup L_f = \{b/1, d/1, f/1\} \\
 L_g &= L_e \cap \overline{L_c} \cup L_g = \{b/1, e/1, g/0\} \\
 L_h &= L_f \cup L_h = \{b/1, d/1, f/1, h/1\} \\
 L_i &= L_f \cup L_i = \{b/1, d/1, f/1, i/1\} \\
 L_j &= L_g \cup L_j = \{b/1, e/1, g/0, j/0\} \\
 L_k &= L_g \cup L_k = \{b/1, e/1, g/0, k/0\} \\
 L_m &= L_h \cap \overline{L_j} \cup L_m = \{d/1, f/1, h/1, m/0\}
 \end{aligned}$$

$$L_n = L_k \cap \overline{L_i} \cup L_n = \{e/1, g/0, k/0, n/0\}$$

$$L_o = L_m \cup L_n \cup L_o = \{d/1, e/1, f/1, g/0, h/1, k/0, m/0, n/0, o/1\}$$

Thus the faults in the final list d/1, e/1, f/1, g/0, h/1, k/0, m/0, n/0, o/1 can be detected with the given vector.

4. (Bushnell and Agrawal) Problem 7.13

Step	Action	Impl. stack	Forward implications	D-frontier
1	Fault act.	$h = 0$	$h = 0, h1 = \overline{D}, i2 = 0$	$i1$
2	D-prop.	$g1 = 1, h = 0$	$g1 = 1, h = 0, h1 = \overline{D}$ $i1 = \overline{D}, i2 = 0$	PO
3	Justify	$e1 = 1, g1 = 1$ $h = 0$	$e1 = 1, g1 = 1, h = 0$ $h1 = \overline{D}, i1 = \overline{D}, i2 = 0$	PO
4	Justify	$a = 1, b = 1$ $e1 = 1, g1 = 1$ $h = 0$	$a = 1, b = 1, e1 = 1, g1 = 1$ $e2 = 1, g1 = 1, g2 = 1$ $h = 0, h1 = \overline{D}, i1 = \overline{D}$ $i2 = 0$	PO
<i>Test found: $(a, b, c, d, h, k) = (1, 1, X, X, 0, X)$; $i1 = \overline{D}$</i>				

The above figure shows the circuit and the signal values specified by D-algorithm.

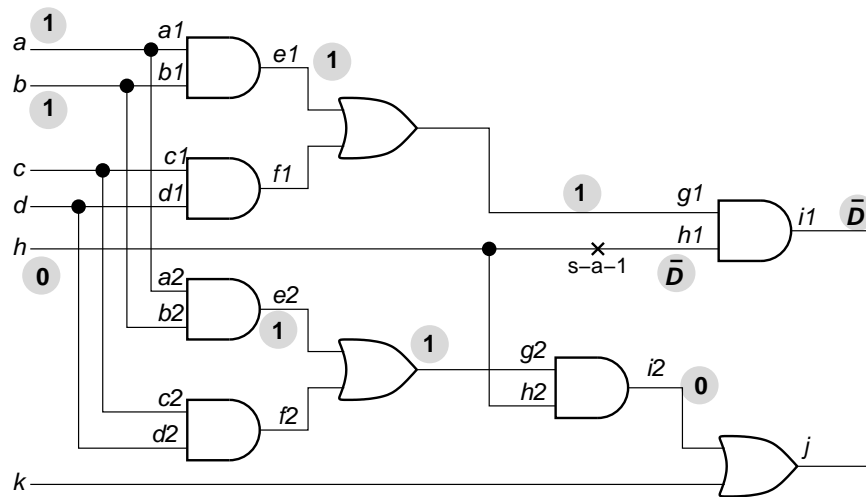


Figure 3: Figure for Problem 5

5. (Bushnell and Agrawal) Problem 7.8

Note : While you are performing the PODEM algorithm, follow the rules given below.

- Order: Try to excite the fault first then propagate.
- Backtrace: Follow a path from the objective to a primary input while always following the alphabetical order (e.g. if a gate has input A and B, backtrace on that gate goes to line A first).
- PI assignment: Always assign 0 first, then assign 1 in case of backtrack.
- Choice of D or D_bar : Always try to propagate a D or D_bar from the D-frontier which has the shortest path to the primary output.
In the case of tie, follow the alphabetical order.

The following table gives the steps of PODEM (see Problem 7.5 for an explanation of *X-path*, it's not required):

Step No.	Objective	Action	Imp. stack	Implied signal values <i>ABCDEFghklmpqsrwZ</i>	<i>D</i> front.	<i>X</i> path
1	$g = 0(\overline{D})$	Backtrace	$C = 0$	$C = 0, h = 0$	ϕ	ok
2	$g = 0(\overline{D})$	Backtrace	$D = 0$ $C = 0$	$C = 0, D = 0, g = 0(\overline{D})$ $h = 0, k = 0, m = 0, u = 0$	ϕ	none
3	$g = 0(\overline{D})$	Backtrack	$D = 1$ $C = 0$	$C = 0, D = 1, g = 1, h = 0$ $k = 1, m = 1, p = 0, q = 1, r = 0$	ϕ	none
4	$g = 0(\overline{D})$	Backtrack	$C = 1$	$C = 1, g = 1, h = 1, m = 1$ $p = 0, q = 1, r = 0$	ϕ	none
5	$g = 0(\overline{D})$	Backtrack	Empty			
<p><i>Algorithm termination: $g = 0(\overline{D})$ with X-path impossible; fault g s-a-1 is redundant. 3 backtracks.</i></p>						

6. A PODEM like test generator is used to generate a test for the fault line v s-a-1 in the circuit shown in Figure 4.

(a) Complete the table below for the test generation process and during the test generation follow the rules given below:

- For this problem, assume that the order of primary input assignments is D, C, B, A, F, then E.
- While backtracing, use the easy/hard heuristic.
- While assigning a value at an input, always assign a 1 before a 0.
- Do not perform x-path check.

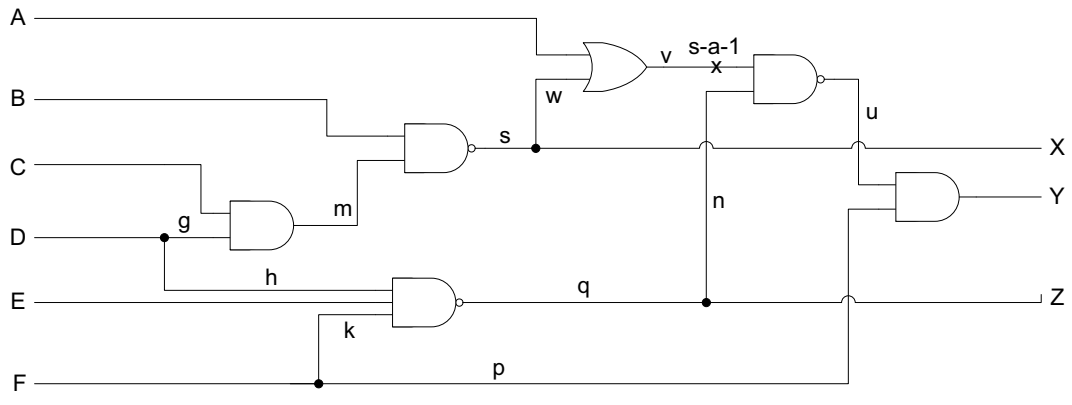


Figure 4: Circuit for Test Generation

In the table fill the necessary entries for each step.

- (b) Construct the decision tree.
- (c) Write the generated test. A B C D E F = **0 1 1 1 0 1**

Step	Objective	Backtrace path	PI assign	D-front	comment
1	v=0	v-w-s-m-g-D	D=1		Objective not satisfied
2	v=0	v-w-s-m-C	C=1		Objective not satisfied
3	v=0	v-w-s-B	B=1		Objective not satisfied
4	v=0	v-A	A=1		failure/backtrack
5	v=0	v-A	A=0	u	fault excited
6	n=1	n-q-F	F=1	u	Objective not satisfied
7	n=1	n-q-E	E=1	u	failure/backtrack
8	n=1	n-q-E	E=0	Y	test found
9					

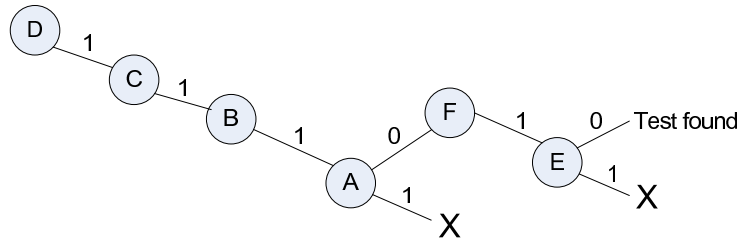
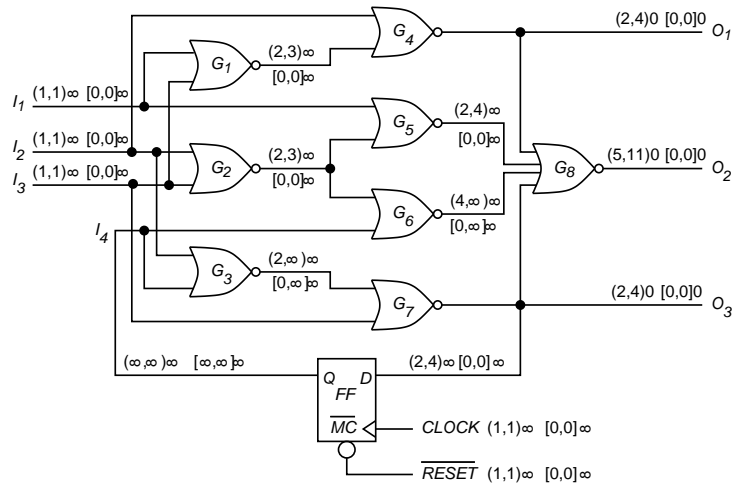


Figure 5: Decision tree

- The steps of calculation for SCOAP testability measures are shown in the three figures that follow. Combinational measures are shown as $(CC0, CC1)CO$ and sequential measures as $[SC0, SC1]SO$.



Circuit of Figure 6.26: PI and PO initialization and first controllability pass.

8. a) Apply the given 10 test vectors to n432 and determine the fault coverage.

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*** SFSP (3-valued) Fault Simulation: Net n432 ***
Total Vectors:      10
Total Fault:        524
Detected Fault:     229
Fault Coverage:     43.70 %
CPU Time:           0.000 seconds
    
```

- b) Use PODEM to generate tests for each fault (without intervening fault simulation). Indicate how many tests are generated and which faults are found to be untestable or aborted. Result can be slightly different depending on backtrack limit you specified for 'podem'. Following statistics are obtained with backtrack limit of 1000000.

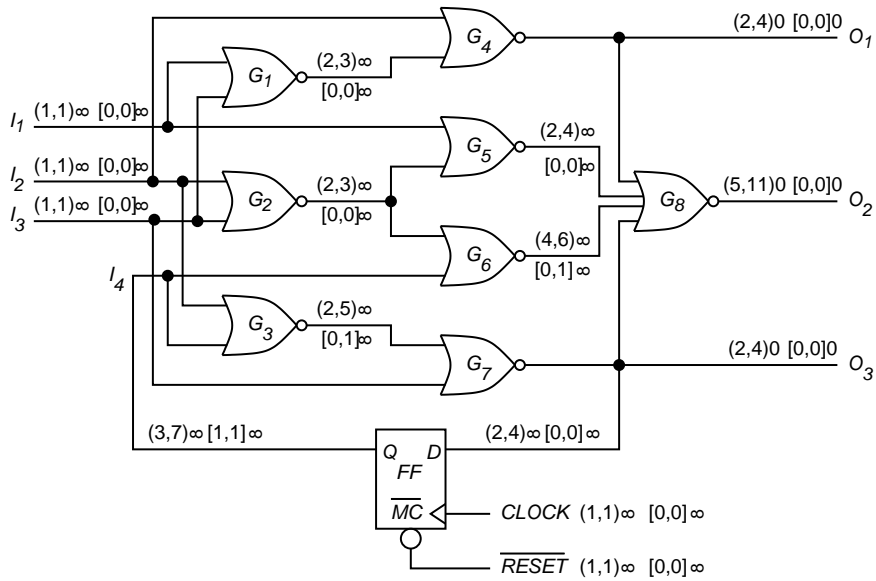
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Total Faults          524
Undetectable faults found 4
Aborted faults        0
Total Time            10 sec.
Time/Fault            0.018384 sec.
Backtracks            2.02574e+06
Implications          4.05777e+06
    
```

Undetected fault list :

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259    0 1
347    0 1
379    0 1
    
```



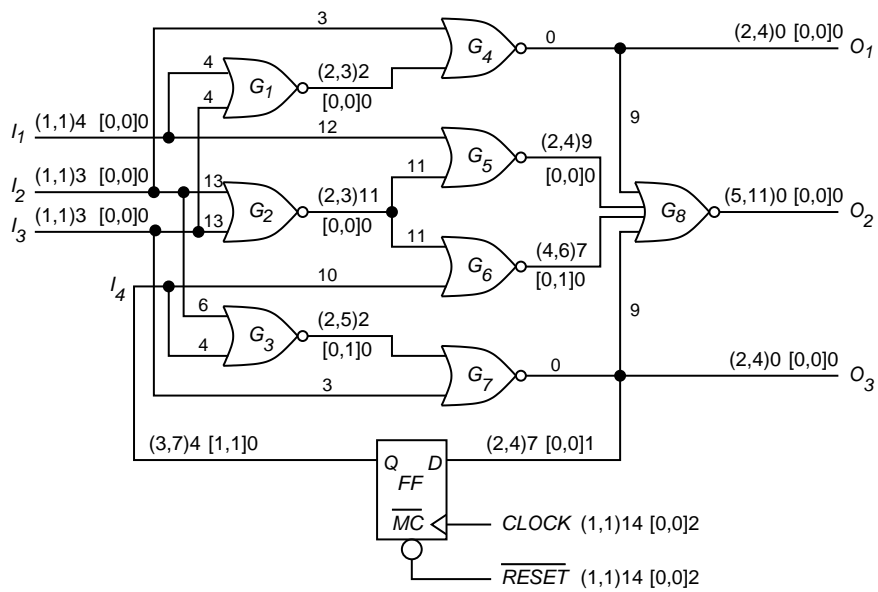
Circuit of Figure 6.26: Converged controllability values.

429 393 1

- c) Choose any 10 test vectors from your list of test vectors, then fill in the X's using 'randvec'. Determine the fault coverage of your 10 vectors and compare that with the coverage of 10 vectors obtained in part (a). Any 10 vectors can be chosen for your answer, following result is only one example.

*** SFSP (3-valued) Fault Simulation: Net n432 ***

Total Vectors:	10
Total Fault:	524
Detected Fault:	241
Fault Coverage:	45.99 %
CPU Time:	0.000 seconds



Circuit of Figure 6.26: All controllability and observability values.