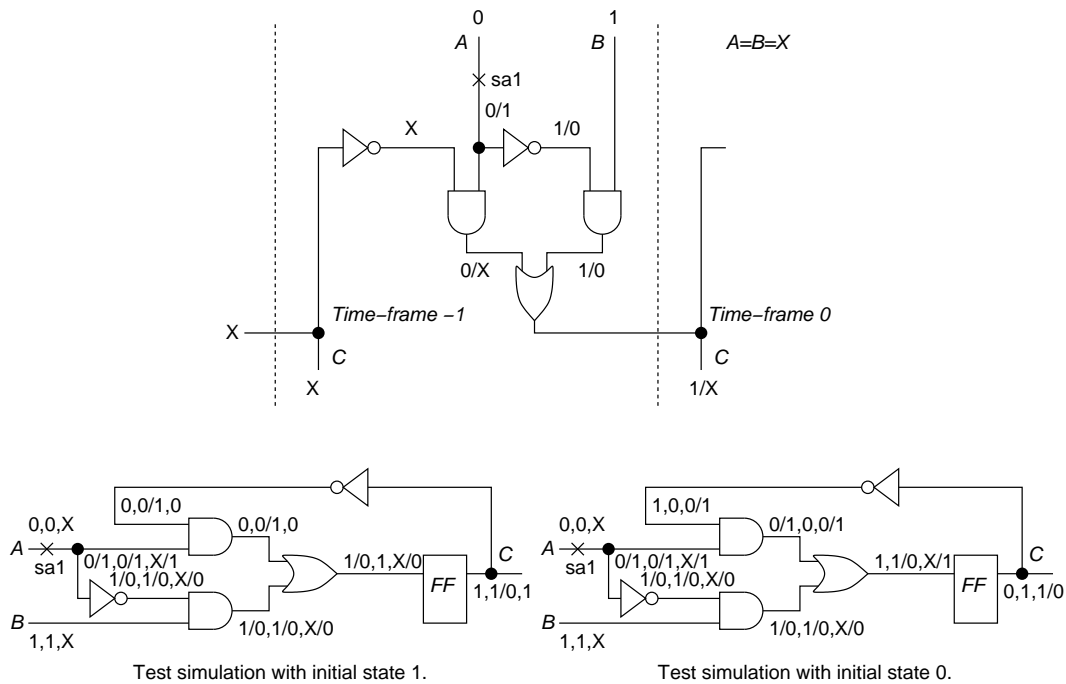


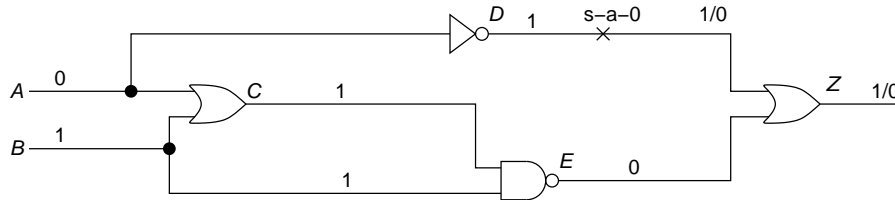
3. (Bushnell and Agrawal) Problem 8.6

The following figure illustrates the time-frame expansion procedure of generating a vector, $A = 0, B = 1$, which starting from the unknown state detects the fault A s-a-1 as $1/X$. After the application of the input vector, the flip-flop is clocked before the output can be observed. Even if we add more vectors to the test sequence, the faulty circuit output will not become deterministic. This is because the faulty circuit is not initializable. The fault is only potentially detectable.

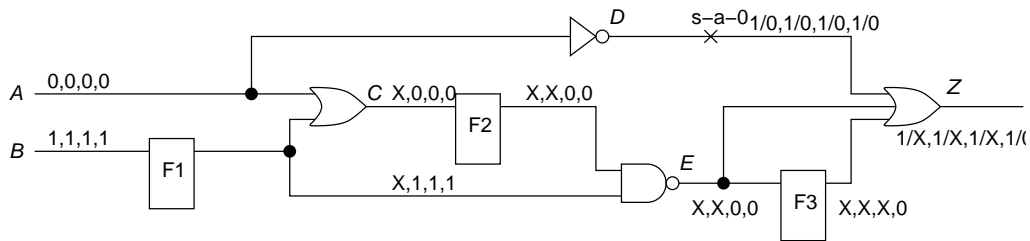


Note: Some test generators will find the potential detection test of the above type. Others will consider the fault untestable (conservative approach.) Most fault simulators will find the fault potentially detectable. Interestingly, the two test simulation scenarios in the figure show that the fault is definitely detectable, though the detection requires multiple observations. If we assume the initial state to be 1 then the fault is detected as $1/0$ after the application of the first clock. However, this output will be 1 (same as the correct output) if the initial state was 0. In this case, repeating the same vector and clocking once again will produce a $1/0$ output. A conventional fault simulator will not report such detection because it does not enumerate the possible initial state scenarios. For such multiple observation tests see reference [525] of the book.

4. The pseudo-combinational circuit and a combinational test, $A = 0, B = 1$, for the fault D s-a-0 are shown in the following figure. Simulation of the sequential circuit with input $A = 0, B = 1$, repeated four times shows that the fault will be detected as 1/0 appearing as the fourth output. We assume that the initial states of all three flip-flops are X .



Pseudo-combinational circuit for the sequential circuit of Figure 8.9..



Test simulation in sequential circuit.

5. The finite state machine $M7$ in Table 1 has a single input, a single output, and 5 states.

a.) It is strongly connected.

b.) You can draw a synchronizing tree and obtain an SS = 0111 1011 1101 1110 and final state will be E.

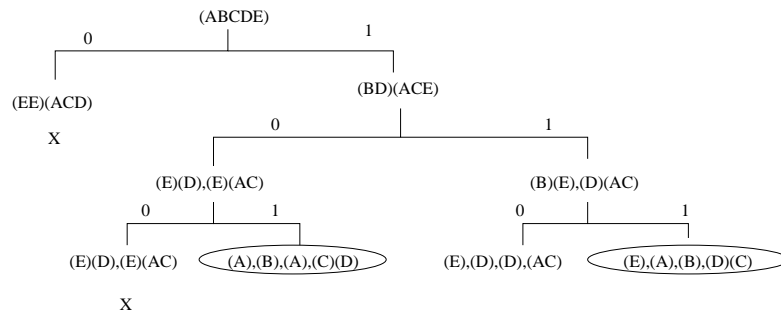
c.) A distinguishing tree is given below and two distinguishing sequences are DS = 101 or 111

DS = 101

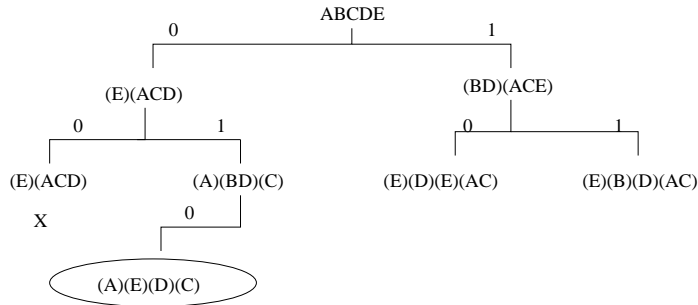
STATE	OUTPUT	FINAL STATE
A	110	D
B	101	A
C	010	B
D	001	A
E	111	C

DS = 111

STATE	OUTPUT	FINAL STATE
A	100	B
B	111	C
C	001	E
D	011	A
E	110	D



d.) The homing tree is given in the figure below and a Homing sequence = 010



6. a) The state machine is given in the tabular form as follows:

Table 1: State Machine for Problem 5.

	Input	
	0	1
A	A/1	B/0
B	E/0	C/1
C	C/1	D/0
D	B/0	A/1
E	A/1	C/0

b) The shortest SS for the given State Machine is : **000101**.

c) There are two shortest length Distinguishing Sequences : **10100** and **10101**. The initial and final states can be tabulated as follows:

DS0 = 10100

DS1 = 10101

Initial	Output	Final	Initial	Output	Final
A	00011	C	A	00010	D
B	11000	E	B	11001	C
C	00111	C	C	00110	D
D	11001	A	D	11000	C
E	01000	E	E	01001	C

