

**Department of Electrical and Computer Engineering
University of Wisconsin–Madison**

**ECE 553: Testing and Testable Design of Digital Systems
Fall 2011**

ASSIGNMENT #5

Date : Thursday, November 10, 2011

Due Date : Tuesday, November 22, 2011

Turn in to TA by 3:00 PM

1. (Pseudo-combinational circuit) For this problem, you need to use a sequential circuit available in

`~ece553/TESTCAD/nets/hw5-circuits/hw5_circuit_1`

- (a) Derive a combinational circuit by replacing each flip-flop (LATCH) to a buffer (BUF). This is known as the pseudo-combinational transformation, which can be applied to any cycle-free clocked sequential circuit.
 - (b) Derive a test for the circuit obtained after (a) for the fault “7 0 0” and “9 0 1”. (You can do this either by hand or by ‘podem’ in the testcad toolset).
 - (c) Verify that the fault “7 0 0” can be detected in the original sequential circuit by repeating the generated vector for three clock cycles.
 - (d) At this point you found that “9 0 1” is redundant in the pseudo-combinational circuit. Now, try to use the sequential test generator (‘fastest’ in testcad toolset) on the original circuit to generate a test vectors for “9 0 1”. Verify if the generated test sequence indeed detects the fault by hand simulation. You’ll find “9 0 1” is not redundant in the original circuit.
 - (e) Explain what causes such a difference between using combinational ATPG on the pseudo-combinational circuit and using sequential test generator on the original sequential circuit.
2. (Sequential test generation using TESTCAD) For this problem, you are required to use ‘fastest’, the sequential test generator in TESTCAD toolset. The sequential circuit under test can be found at the location given below:

`~ece553/TESTCAD/nets/hw5-circuits/hw5_circuit_2`

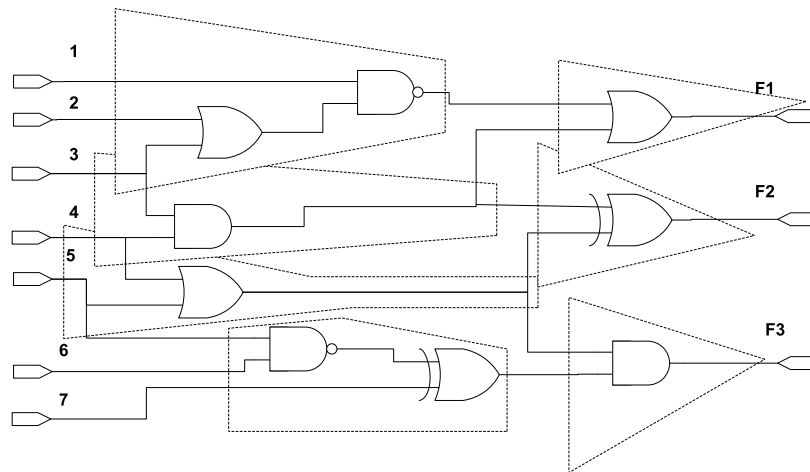


Fig.2

5. (Bushnell and Agrawal) Problem 9.10, do all parts