1. (20 points) (Bushnell and Agrawal) Problem 14.4

Assume 20 equal length scan chains, each having $2000/20 = 100$ flip-flops. Scan sequence test length is given by:

\[
\text{Scan test length} = (n_{\text{comb}} + 2) \times n_{\text{chain}} + n_{\text{comb}} + 4
\]

\[
= (500 + 2) \times 100 + 500 + 4
\]

\[
= 50,704 \text{ clock cycles}
\]

where $n_{\text{comb}}$ = number of combinational vectors, and $n_{\text{chain}}$ = number of flip-flops in the longest scan chain.

Gate Overhead: All scanin inputs are obtained as fanouts of normal PIs. A multiplexer is inserted between each PO and its normal output signal. The other data input of the multiplexer is a scanout and control is the test control (TC) PI. Assuming normal data flip-flops of 10 gates, the overheads are:

\[
\text{Overhead (single chain)} = 4n_{sff} + 4 = 4 \times 2000 + 4 = 8,004 \text{ gates}
\]

\[
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\]

where $n_{sff}$ = total number of scan flip-flops. A multiplexer is assumed to have 4 gates. Only one multiplexer is added for the scanout.

Extra overhead (20 chains) = $4(N_{\text{chain}} - 1) = 4 \times 19 = 76$

Total gates in pre–scan circuit = $100,000 + 10n_{ff} = 120,000$

where $n_{ff}$ = total number of flip-flops.

Extra overhead of 20 chains = $\frac{76}{120,000 + 8,004} \times 100 = 0.06\%$

An overhead of 0.06% is incurred to reduce the test length by a factor of $\sim 20$. 

Fall 2014 (Lec: Saluja)
2. (20 points) Consider the figure 14.16 in the textbook. Draw the S-graph for the circuit and identify the flip-flop to be scanned so that all cycles are broken. Redraw the circuit with the scan circuitry and also draw the circuit that will be used by a test generator for the circuit with scan.

The s-graph of the circuit in Figure 14.16 is given in Figure 1.

![S-graph of the Circuit](image1)

Figure 1: S-graph of the Circuit

**By scanning F1 all cycles can be eliminated.**

The partial-scan circuit is given below in Figure 2. Added circuitry is shown in grey and wiring, in bold lines. We insert a multiplexer at the input of F1. One input of this multiplexer is the normal input of F1. The other input is a fanout of PI I, which is now also used as SCANIN. The control input of the multiplexer is a new PI, TC. TC = 0 is scan mode and TC = 1 is the normal mode. TC = 0 also inhibits the clocking of the non-scan flip-flop F2 such that it holds its state during the scan operation. This is accomplished by using the grey-shaded AND gate. PO Z also acts as SCANOUT.

![Partial-scan design of the Circuit](image2)

Figure 2: Partial Scan Circuit

The ATPG circuit is obtained by removing the MUX and F1, making Z a new PI SCANIN, and making the AND gate output feeding into the MUX a new PO.
SCANOUT_Z.

Figure 3: Circuit used by ATPG tool.

The circuit is shown in figure 3.
3. (20 points) (Bushnell and Agrawal) Problem 15.2.

Is the polynomial generated reducible or irreducible? If it is reducible, give its factors.

The implementation of polynomial in a standard LFSR is shown in the figure:

\[ f(x) = x^8 + x^7 + x^2 + 1 \]

This polynomial is reducible. One of its factors is \( x + 1 \). In fact

\[ x^8 + x^7 + x^2 + 1 = (x + 1)(X^7 + x + 1) \]

and \( x^7 + x + 1 \) is not factorable.
4. (20 points) (Bushnell and Agrawal) Problem 15.13.
A standard LFSR and its patterns are shown below.

The next figure gives an augmented LFSR and the patterns it produces. This definitively uses less hardware than a counter, which needs more complex gates. It gets comparatively simpler as the counter width increases. A counter and its patterns are also shown below.
5. (20 points) (Bushnell and Agrawal) Problem 15.16, only do faults f s-a-0 and B-g s-a-0.

Solution below is for all faults in the text problem.

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6. (not for credit but must do problem) (Bushnell and Agrawal) Problem 16.3

Each chip has a boundary scan register. It takes 5 clocks to go from shift-DR through update-DR and back to shift-DR.

**First scenario:**

\[
\text{Pattern shift – in time} = \text{shift – out time} = 1024 + 512 + 1024 + 512 = 3072
\]

\[
\text{Total test time} = \frac{\text{Chip 1 time + Chip 2 time} + \text{Chip 3 time} + \text{Chip 4 time}}{\text{clock}} = \frac{500,000(\text{shift time} + 5) + \text{shift time} + 1,000,000(\text{shift time} + 5) + \text{shift time} + 1,000,000(\text{shift time} + 5) + \text{shift time} + 500,000(\text{shift time} + 5) + \text{shift time}}{\text{clock}}
\]

However, three of the extra shift times can be eliminated by overlap of scan out with scan in as testing shifts from one chip to the next one.

\[
\text{Total test time} = \frac{3,000,000 \times 3,077 + 3,072}{512 \text{ MHz}} = 18.0293 \text{ s}
\]

**Second scenario with bypass register:**

\[
\begin{align*}
\text{Chip 1 shift time} & = 1027 \\
\text{Chip 2 shift time} & = 515 \\
\text{Chip 3 shift time} & = 1027 \\
\text{Chip 4 shift time} & = 515 \\
\text{Total test time} & = \frac{500,000(1027 + 5) + 1027 + 1,000,000(515 + 5) + 515 + 1,000,000(1027 + 5) + 1027 + 500,000(515 + 5) + 515}{512 \text{ MHz}} \\
& = 4.54688 \text{ s}
\end{align*}
\]
To be really thorough, we should add the time to change test instructions. Let us assume a 6-bit instruction register. Then,

\[
\text{Test instruction change time} = \frac{(3 + 24 \times 1 + 3)}{\text{clock}} \\
\text{(See Figure 16.11 TAP controller state diagram)} \\
= \frac{30}{(512 \text{ MHz})} = 5.859375 \times 10^{-8} \text{s}
\]

Updated times with instruction changes:

**First scenario:**

\[
\text{Test time} = \text{Prior test time} + 1 \text{ instruction change} \\
= 18.0293 + 5.859375 \times 10^{-8} \text{ s} = 18.0293 \text{ s}
\]

**Second scenario:**

\[
\text{Test time} = \text{Prior test time} + 4 \text{ instruction changes} \\
= 4.54688 + 5.859375 \times 10^{-8} \text{ s} = 4.54688 \text{ s}
\]

So, test instruction changing time is negligible for large chips.