

2. Consider the following RAM test algorithm.

$\uparrow (W0) \uparrow (R0, W1, R1) \uparrow (R1, W0, R0)$

- (a) Which of the following two-coupling faults will be detected or not-detected by this test assuming that RAM contains 1M cells.

-A change in the contents of cell 600 causes cell 10005 to change

This fault will be excited at the W1 the second march (M2-W1), and will be detected at M2-R0.

-A change in the cell content 30018 causes cell 0 to change

This fault will be excited at M2-W1, and will be detected at M3-R1.

- (b) Identify all two-coupling faults from six different cases shown below that will not be detected by the above test algorithm.

Note: For each of the following faults, there are two cases as $(i < j)$ and $(j < i)$, and we have ignored all initial condition related effects.

- a \uparrow transition in i causes \uparrow transition in j

$(i < j)$:

Excited at M2-W1, Detected at M2-R0

$(j < i)$:

Excited at M2-W1, Not detected

- a \uparrow transition in i causes \downarrow transition in j

$(i < j)$:

Never excited, Not detected

$(j < i)$:

Excited at M2-W1, Detected at M3-R1

- a \downarrow transition in i causes \uparrow transition in j

$(i < j)$:

Not excited. Not detected.

$(j < i)$:

Excited in M3-W0, but never read, so not detected.

Note: Potentially excited at M1-W0, so potentially detected at M2-R0

- a \downarrow transition in i causes \downarrow transition in j

$(i < j)$:

Excited at M3-W0, Detected at M3-R1

$(j < i)$:

Not excited. Not detectable.

- a \uparrow transition in i causes \uparrow transition in j

($i < j$):

Excited at M2-W1, Detected at M2-R0

($j < i$):

Excited at M2-W1, Detected at M3-R1

- a \downarrow transition in i causes \downarrow transition in j

($i < j$):

Excited at M3-W0, Detected at M3-R1

($j < i$):

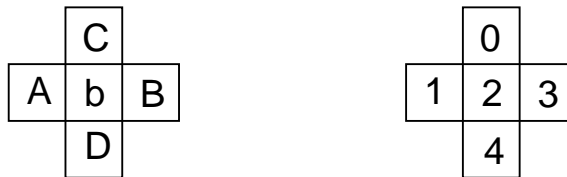
Excited at M3-W0, Not detectable.

3. (Bushnell and Agrawal) Problem 9.22

We write the steps (in pseudo-code) for a test to detect the passive neighborhood pattern sensitive faults (PNPSF),

$$\langle 1, 0, 1, 0; \uparrow / 0 \rangle \text{ and } \langle 0, 1, 0, 1; \downarrow / 1 \rangle$$

using the two-group method and type-1 neighborhood. The test need not be the optimal one.



Write '0' to base cell;

Write "1010" to cells 0, 1, 3, 4;

Write '1' to base cell;

Read base cell (test fails in it is '0');

Write '1' to base cell;

Write "0101" to cells 0, 1, 3, 4; Write '0' to base cell;

Read base cell (test fails in it is '1');

4. (Bushnell and Agrawal) Problem 13.1

Examining Figure 13.12(c), we see that rows $i = 1, 2,$ and 4 of the leakage fault table cover all possible tests. We need these stuck-fault vectors:

I_1	I_2	O_1	
0	0	1	$i = 1$
0	1	0	$i = 2$
1	0	0	$i = 4$

5. (Bushnell and Agrawal) Problem 14.4

Assume 20 equal length scan chains, each having $2000/20 = 100$ flip-flops. Scan sequence test length is given by:

$$\begin{aligned} \text{Scan test length} &= (n_{comb} + 2) \times n_{chain} + n_{comb} + 4 \\ &= (500 + 2) \times 100 + 500 + 4 \\ &= 50,704 \text{ clock cycles} \end{aligned}$$

where n_{comb} = number of combinational vectors, and n_{chain} = number of flip-flops in the longest scan chain.

Gate Overhead: All scanin inputs are obtained as fanouts of normal PIs. A multiplexer is inserted between each PO and its normal output signal. The other data input of the multiplexer is a scanout and control is the test control (TC) PI. Assuming normal data flip-flops of 10 gates, the overheads are:

$$\text{Overhead (single chain)} = 4n_{sff} + 4 = 4 \times 2000 + 4 = 8,004 \text{ gates}$$

where n_{sff} = total number of scan flip-flops. A multiplexer is assumed to have 4 gates. Only one multiplexer is added for the scanout.

$$\text{Extra overhead (20 chains)} = 4(N_{chain} - 1) = 4 \times 19 = 76$$

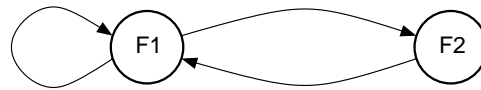
$$\text{Total gates in pre - scan circuit} = 100,000 + 10n_{ff} = 120,000$$

where n_{ff} = total number of flip-flops.

$$\text{Extra overhead of 20 chains} = \frac{76}{120,000 + 8,004} \times 100 = 0.06\%$$

An overhead of 0.06% is incurred to reduce the test length by a factor of ~ 20 .

6. Consider the figure 14.16 in the the textbook. Draw the S-graph for the circuit and identify the flip-flop to be scanned so that all cycles are broken. Redraw the circuit with the scan circuitry and also draw the circuit that will be used by a test generator for the circuit with scan.



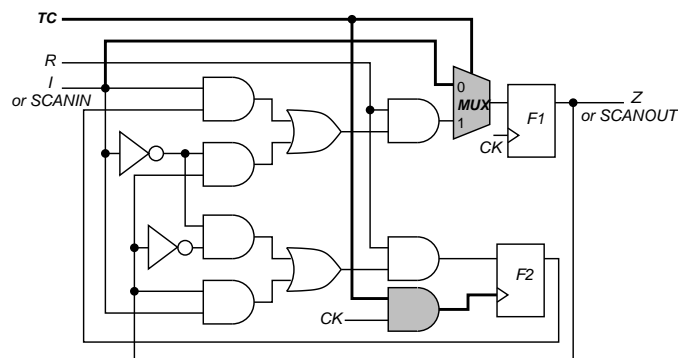
s-graph for the circuit of Figure 14.16.

Figure 1: S-graph of the Circuit

The s-graph of the circuit in Figure 14.16 is given in Figure 1.

By scanning F1 all cycles can be eliminated.

The partial-scan circuit is given below in Figure 2. Added circuitry is shown in grey and wiring, in bold lines. We insert a multiplexer at the input of F1. One input of this multiplexer is the normal input of F1. The other input is a fanout of PI I , which is now also used as $SCANIN$. The control input of the multiplexer is a new PI, TC . $TC = 0$ is scan mode and $TC = 1$ is the normal mode. $TC = 0$ also inhibits the clocking of the non-scan flip-flop $F2$ such that it holds its state during the scan operation. This is accomplished by using the grey-shaded AND gate. PO Z also acts as $SCANOUT$.

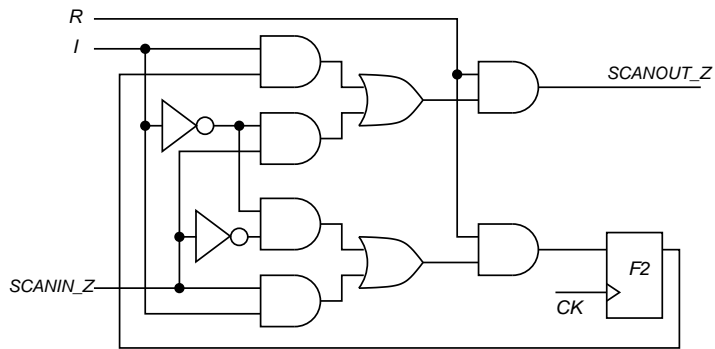


Partial-scan design of the circuit of Figure 14.16.

Figure 2: Partial Scan Circuit

The ATPG circuit is obtained by removing the MUX and $F1$, making Z a new PI $SCANIN_Z$, and making the AND gate output feeding into the MUX a new PO $SCANOUT_Z$.

The circuit is shown in figure 3.



ATPG circuit for the partial-scan design of the circuit of Figure 14.16.

Figure 3: Circuit used by ATPG tool.