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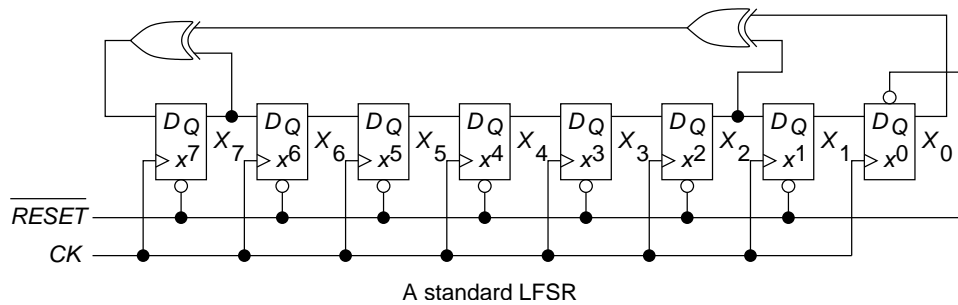
ECE 553: Testing and Testable Design of Digital Systems
 Fall 2011

ASSIGNMENT #7
Solution

1. (Bushnell and Agrawal) Problem 15.2

Consider the polynomial for a standard LFSR shown in the figure:

$$f(x) = x^8 + x^7 + x^2 + 1$$



$$\mathbf{X}(t+1) = \mathbf{T}_s \mathbf{X}(t)$$

$$\begin{bmatrix} X_0(t+1) \\ X_1(t+1) \\ X_2(t+1) \\ X_3(t+1) \\ X_4(t+1) \\ X_5(t+1) \\ X_6(t+1) \\ X_7(t+1) \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} X_0(t) \\ X_1(t) \\ X_2(t) \\ X_3(t) \\ X_4(t) \\ X_5(t) \\ X_6(t) \\ X_7(t) \end{bmatrix}$$

3. (Bushnell and Agrawal) Problem 15.16

ABC	Good $R_1R_2R_3$	B s-a-0		B s-a-1		$B - g$ s-a-0	
		YZ	Bad $R_1R_2R_3$	YZ	Bad $R_1R_2R_3$	YZ	Bad $R_1R_2R_3$
001	000	11	000	01	000	11	000
100	011	10	011	10	001	10	011
010	011	10	011	10	110	11	011
101	011	11	011	11	101	11	010
110	010	10	010	10	101	11	110
111	111	11	111	11	100	10	100
011	000	11	000	01	001	01	000
001	001	11	011	01	101	11	001
	111		010 Yes		111 No		111 No

ABC	Good $R_1R_2R_3$	$B - g$ s-a-1		f s-a-0		f s-a-1	
		YZ	Bad $R_1R_2R_3$	YZ	Bad $R_1R_2R_3$	YZ	Bad $R_1R_2R_3$
001	000	10	000	00	000	11	000
100	011	11	010	00	000	10	011
010	011	10	110	01	000	10	011
101	011	10	101	00	001	11	011
110	010	10	100	01	100	10	010
111	111	11	000	01	011	11	111
011	000	01	011	01	000	11	000
001	001	10	000	00	001	11	011
	111		010 Yes		100 Yes		010 Yes

4. (Bushnell and Agrawal) Problem 16.3

Each chip has a boundary scan register. It takes 5 clocks to go from shift-DR through update-DR and back to shift-DR.

First scenario:

$$\begin{aligned} \text{Pattern shift - in time} &= \text{shift - out time} \\ &= 1024 + 512 + 1024 + 512 = 3072 \end{aligned}$$

$$\begin{aligned} \text{Total test time} &= [\text{Chip 1 time} + \text{Chip 2 time} \\ &\quad \text{Chip 3 time} + \text{Chip 4 time}]/\text{clock} \\ &= [500,000(\text{shift time} + 5) + \text{shift time} \\ &\quad + 1,000,000(\text{shift time} + 5) + \text{shift time} \\ &\quad + 1,000,000(\text{shift time} + 5) + \text{shift time} \\ &\quad + 500,000(\text{shift time} + 5) + \text{shift time}]/\text{clock} \end{aligned}$$

However, three of the extra shift times can be eliminated by overlap of scan out with scan in as testing shifts from one chip to the next one.

$$\begin{aligned} \text{Total test time} &= [3,000,000 \times 3,077 + 3,072]/512 \text{ MHz} \\ &= \boxed{18.0293 \text{ s}} \end{aligned}$$

Second scenario with bypass register:

$$\begin{aligned} \text{Chip 1 shift time} &= 1027 \\ \text{Chip 2 shift time} &= 515 \\ \text{Chip 3 shift time} &= 1027 \\ \text{Chip 4 shift time} &= 515 \\ \text{Total test time} &= [500,000(1027 + 5) + 1027 \\ &\quad + 1,000,000(515 + 5) + 515 \\ &\quad + 1,000,000(1027 + 5) + 1027 \\ &\quad + 500,000(515 + 5) + 515]/512 \text{ MHz} \\ &= \boxed{4.54688 \text{ s}} \end{aligned}$$

To be really thorough, we should add the time to change test instructions. Let us assume a 6-bit instruction register. Then,

$$\begin{aligned}\text{Test instruction change time} &= (3 + 24 \times 1 + 3)/\text{clock} \\ &\quad (\text{See Figure 16.11 TAP controller state diagram}) \\ &= 30/(512 \text{ MHz}) = \boxed{5.859375 \times 10^{-8} \text{ s}}\end{aligned}$$

Updated times with instruction changes:

First scenario:

$$\begin{aligned}\text{Test time} &= \text{Prior test time} + 1 \text{ instruction change} \\ &= 18.0293 + 5.859375 \times 10^{-8} \text{ s} = 18.0293 \text{ s}\end{aligned}$$

Second scenario:

$$\begin{aligned}\text{Test time} &= \text{Prior test time} + 4 \text{ instruction changes} \\ &= 4.54688 + 5.859375 \times 10^{-8} \text{ s} = 4.54688 \text{ s}\end{aligned}$$

So, test instruction changing time is negligible for large chips.