

**Department of Electrical and Computer Engineering
University of Wisconsin–Madison**

**ECE 553: Testing and Testable Design of Digital Systems
Fall 2011**

Project - Test Generation, Diagnosis, and Partial Scan

Date: **November 11, 2011** (Friday)
Final Due Date: **December 8, 2011** (Thursday)
Weight: 20 - 25%

Deadlines: Please note all deadlines given below.

- Nov 11, Thursday: Project distribution - project details are made available.
- Nov 16, Wednesday: Decide Teams and email TA.
- Nov 17, Thursday: Circuit assignment (Part I and II). You will hear from the TA by 5:00 PM.
- Nov 24, Thursday: Progress and Status Report Due (1 page only). Hand over the following to the TA:
 - Part I: Test statistics (coverage, number of vectors, and first 10 test vectors)
 - Part II: The test coverages for the original circuit, fully scanned circuit, and partially scanned (6 scanable FFs) circuit.
- Dec 8, Tuesday: Final report due (Part I and II) 5:00 PM.

Overview:

For the project, you will be working **as a group of two students**.

There are two parts to the project, namely the detect/diagnose (part I) and the partial scan (part II).

For the detection and diagnosis part, you are required to develop a complete test set for a given circuit by using the tools described in the ATPG Tool Set. The test set developed must be economical but need not be absolutely minimum in size. You are encouraged to explore different test pattern generation strategies, such as using random test patterns, functional test patterns as seeds, or a priori determining the number of vectors you will generate before performing fault simulation.

After obtaining the test set, you will be given **Three** circuits (virtual chips, presumably realizations of the circuit for which you generated tests). Use your test set to determine if the circuits are faulty or fault-free. You should find one or more of the three circuits to be faulty. For the faulty circuits, you are required to perform diagnosis to locate the fault for one of the faulty circuits.

The grade for the project will depend on the size of the test set for fault detection and for fault diagnosis, the fault coverage, the performance of test strategies, test case results, and the final report. Note that it is possible that you may have to generate additional tests to improve diagnostic resolution.

For the partial scan insertion part, you need to identify all the flip-flops that are included in feedback cycle(s). Then you are allowed to scan up to six flip-flops to increase testability of your circuit. This part will be graded based on the strategy to select flip-flops and the fault coverage obtained by 'fastest'.

Part I: Combinational Test Generation (75% weight of the project)

1. **Test Generation for circuit to be tested:**

Each one of you will be provided its own circuit. All the circuits will have the same number of primary inputs, outputs, and the number of gates. All circuits are expected to have the same test generation complexity. However, this does not mean that all the circuits are identical.

2. **Testing the circuits (Virtual Chips):**

You will be given **Three** additional versions of your circuit. Apply your test set to find one or more faulty circuits among these circuits. Once you identify the faulty circuits, you are required to perform diagnosis to determine the location of the fault for the fault circuit with lowest index. (e.g. if you find circuits v-chip-2 and v-chip-3 are faulty, then perform fault diagnosis on circuit v-chip-2.) Due to the fault equivalence and your possible use of fault dominance during test generation phase, there might be more than one answer and your diagnosis may not be perfect. However, the goal is to determine smallest set of possible candidate faults. If this requires generation of additional tests or establishing further equivalences, please do so.

Part II: Partial scan (25% weight of the project)

Each one of you will be provided your own sequential circuit. As before, all circuits are of similar complexity and similar statistics. Your first goal is to find six flip-flops that are included in feedback cycles. Once you identify those flip-flops, your next goal is to find a set of no more than 6 flip-flops to achieve maximum coverage that you can

get. For this part you are required to use 'fastest' to generate tests and to check the fault coverage.

Final Report:

You will submit a written report and an on-line report. The written report should contain two parts - result and discussion for both Combinational test generation and for partial scan.

For part I (Combinational test generation and diagnosis), the result part should include the total number of tests, fault coverage, a report on undetected faults, test results on **Three** circuits (virtual chips), and diagnosis result on the faulty circuit with lowest index.

For part II (Partial scan), the results should contain 1) test statistics with/without scan, 2) six flip-flops that are included in the feedback cycle(s), and 3) six flip-flops you chose to scan to achieve maximum fault coverage.

In discussion parts, you should include the originally planned strategies and the final strategies you used for each part, i.e, for test generation, diagnosis, and scan flip-flop selection. You should also discuss the effectiveness of your strategies, the difficulties you encountered, and make suggestions for avoiding such difficulties or suggest more effective strategies.

The on-line report should include all files that you created: programs or scripts containing your test set, coverage statistics results for your test set, diagnosis related files, and partial scan related files. You will be informed by the TA as to how and when to submit these files. Meanwhile prepare the the following. Under your group directory, prepare 3 sub-directories, namely REPORT, PART_I and PART_II. Each sub-directory should contain:

- REPORT : Copy of your written report
- PART_I : Files used for PART_I of the project.
- PART_II : Files used for PART_II of the project.

You must also prepare a **Readme** file in this directory, or in every subdirectory, explaining the contents of the directory. To avoid penalty or last minute problems, you are advised to put everything in place well before the due date, but do not give others read permission on the files. The method of submission for the on-line report will be announced later by an email from the TA.

The written report should follow the format and outline given below:

1. Names of the Members of the group:

2. Group number assigned to you:
3. *Part I: Detection/Diagnosis Test Generation*
 - (a) Problem Statement(s): (no more than 4 lines)
 - (b) Result:
 - i. Total number of tests
 - ii. Fault Coverage
 - iii. List of undetected/undetectable faults
 - iv. The test result for three circuits
 - v. The diagnosis result on faulty circuit with lowest index
 - vi. Every 15th test vector from the set of first 100 vectors
 - (c) Test Generation: (no more than 2 pages)
 - i. The originally planned strategy
 - ii. The actual strategy used
 - iii. The details of the test generation process
 - iv. Discussion
 - (d) Fault Diagnosis: (no more than 2 pages)
 - i. The originally planned strategy
 - ii. The actual strategy used
 - iii. The details of the diagnosis process
 - iv. Discussion and Comments

Part II: Partial scan

1. Problem Statement(s): (no more than 4 lines)
2. Result: (no more than 3 pages)
 - (a) Statistics for unmodified circuit
 - (b) Six flip-flops that are included in feedback cycle(s)
 - (c) Strategies for selecting scan flip-flops
 - (d) Selected set of flip-flops
 - (e) Statistics for partially scanned circuit
 - (f) Discussion and Comments (no more than $\frac{1}{2}$ page)

Use of flowcharts or pseudo-codes in describing strategies is highly recommended. The written report is to be typed and spell-checked using any word-processing softwares of your choice. Please use $8\frac{1}{2} \times 11$ inch pages for the report with 1 1/2 line spacing and point size no smaller than 10. *Figures and computer outputs, if included with the report, must also fit into the $8\frac{1}{2} \times 11$ inch page size and in the page limit specified.*