The Xilinx Virtex Series FPGA

• Virtex FPGA Structure
• Specific Features
  – IOB
  – CLB - Function Generators, Flip-Flops, SRAM, and Fast Carry Logic
  – Three-State Buffers
  – Block SelectRAM
  – Programmable Routing Matrix
  – Clock Distribution (Delay-Locked Loops)
  – Boundary Scan
  – Configuration
• Virtex XCV800-PQ/HQ240 C Characteristics

Virtex FPGA Architecture

• Primary Reference:
• See Figure 1: Virtex Architecture Overview
  – IOBs - Input/Output Blocks
  – CLBs - Configurable Logic Blocks
  – GRM - General Routing Matrix
  – 3-state buffers
  – BRAMs - Block SelectRAM
  – DLLs - Delay-Locked Loops
  – VersaRing - I/O interface routing resources
Virtex FPGA Architecture

- Logic configured by values stored in SRAM cells
  - CLBs implement logic in SRAM-stored truth tables
  - CLBs use SRAM-controlled multiplexers
  - Routing uses “pass” transistors for making/breaking connections between wire segments
- See Table 1: Virtex FPGA Family Members
Table 1 – Virtex FPGA Family Members

<table>
<thead>
<tr>
<th>Device</th>
<th>System Gates</th>
<th>CLB Array</th>
<th>Logic Cells</th>
<th>Maximum Available I/O</th>
<th>Block RAM Bits</th>
<th>Maximum SelectRAM™ Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCV50</td>
<td>57,905</td>
<td>16x24</td>
<td>1,728</td>
<td>180</td>
<td>32,768</td>
<td>24,576</td>
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<td>512</td>
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<td>131,072</td>
<td>393,216</td>
</tr>
</tbody>
</table>

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IOB - Input/Output Block

- See Figure 2: Virtex Input/Output Block
- Output Features
  - Optional data output D flip-flop with clock enable and shared asynchronous Set/Reset
  - Optional 3-state control D flip-flop with clock enable and shared asynchronous Set/Reset
  - Three-state output buffer
  - Independent polarity controls on output buffer and control signals

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IOB - Input/Output Block

- Output Features (continued)
  - Electrostatic discharge (ESD) (protection)
  - Optional pull-up and pull-down resistors (note comments in documentation on state of pull-ups and pull-down during configuration)
  - Weak keeper circuit
  - Wide range of low-voltage signaling standards (See Table 3).
  - Strong current drive (24 ma source, 48 ma sink)
  - Drive strength and slew rate controls
IOB - Input/Output Block

- Input Features
  - Input Buffer
  - Wide range of low-voltage signaling standards
  - Programmable delay for forcing pad-to-pad hold time to zero
  - Optional data D flip-flop with clock enable and shared Set/Reset
  - Optional pull-up and pull-down resistors (Same ones as for output use)

CLB - Configurable Logic Block

- See Figure 4: 2-Slice Virtex CLB
- Contains two logic cells
- Each logic cell contains:
  - 2 Look-up tables (LUTs)
  - 2 D flip-flops/latches
  - Fast carry logic
  - Three-state drivers
  - SRAM control logic
CLB - Configurable Logic Block

- See Figure 5: Detailed View of Virtex Slice
- Logic Function Implementation
  - 2 Function Generators - Each a 4-input LUT - implements any 4-input function
  - F5 multiplexer - combines two LUTs with select input - implements any 5-input function, 4-to-1 mux, or selected functions of up to 9 inputs.
  - F6 multiplexer - combines outputs of two F5 multiplexer - implements any 6-input function, 8-to-1 mux, or selected functions of up to 19 inputs.
  - Four direct feedthrough paths - useful to facilitate routing by use of through-the-cell paths
CLB - Configurable Logic Block

- Storage Elements
  - 2 D flip-flops/latches
  - Optionally included in cell output paths
  - Shared clock enable
  - Shared synchronous/asynchronous Set/Reset signals
    - SR - forces storage element into initialization state specified
    - BY - forces storage element into opposite state
  - All control signals independently invertible
CLB - Configurable Logic Block

• Fast Carry Logic (See Figure 5)
  – Two chains of two bits per CLB
  – AND gate, 0/1 Mux, CY Mux, EXOR
  – Manchester Carry Chain-Like

• 3-state Drivers (BUFT) - on-chip drivers with independent control (T and E) and input pins

• Distributed LUT SelectRAMs - Per logic cell, one of:
  • Two 16 x 1-bit synchronous RAM
  • 16 x 2-bit synchronous RAM
  • 32 x 1-bit synchronous RAM
  • 16 x 1 dual-port synchronous RAM
  • Two 16-bit shift registers

Block SelectRAM

• Fully synchronous dual-ported 4096-bit RAM
  – Stores address, data and write-control signal on inputs
  – Cannot change address, even for read without using clock
  – For dual port use, interesting timing restrictions
  – See App Note XAPP130 http://www.xilinx.com/xapp/xapp130.pdf

• Organized in vertical columns of blocks on left and right of CLB array
• Block height is 4 CLBs => Number of block per column is (height of CLB of array)/4

• See Table 3: Virtex Block SelectRAM Amounts
• See Figure 6: Dual-Port Block SelectRAM
• Independent control signals for each port
• See Table 4: Block SelectRAM Port Aspect Ratios
• Ratios independently selectable
Programmable Routing Matrix

- Local Routing
  - See Figure 7: Virtex Local Routing
  - Interconnections among LUTs, flip-flops, and General Routing Matrix (GRM)
  - Internal CLB feedback paths that can chain LUTs together
  - Direct paths between horizontally-adjacent CLBs
  - Short connections with few “pass” transistors => low delay => high-speed connections
Programmable Routing Matrix

- General Purpose Routing
  - Majority of interconnect resources
  - In horizontal and vertical routing channels associated with rows and columns of CLBs
  - GRM - Switch matrix through which horizontal and vertical routing resources connect and means by which CLBs access general purpose routing
    - 24 single-length lines between adjacent GRMs in 4 directions
    - 72 buffered hex lines route GRM signals to other GRMs 6 blocks away in 4 directions
    - 12 longlines are buffered bidirectional wires that distribute signals across the device
      - Vertical - span full device height
      - Horizontal - span full device width
Programmable Routing Matrix

- I/O Routing
  - VersaRing
  - Supports pin-swapping and pin-locking
  - Facilitates pin-out flexibility for concurrent connecting component design

- Dedicated Routing
  - Four partitionable bus lines per CLB row driven by BUFTs (See Figure 8: BUFT Connections)
  - Two dedicated nets per CLB for vertical carry signals to adjacent cells

Figure 8: BUFT Connections
Programmable Routing Matrix

- Global Routing
  - Distribute Clocks and other signals with high fanout
  - Primary Global Routing
    • Four dedicated global nets with dedicated input pins for clocks
    • Driven by global buffers
  - Secondary Global Routing
    • 24 backbone lines, 12 across top of chip and 12 across bottom of chip
    • From these, can distribute 12 unique signals/column via 12 longlines in column
    • Not restricted to routing only clock pins

Clock Distribution

- Via primary global routing resources
- See Figure 9: Global Clock Distribution Network
- Four global buffers
  - Two at top center
  - Two at bottom center
- Four dedicated clock input pads
- Input to global buffers from pads or from general purpose routing
Delay-Locked Loops (DLLs)

• One associated with each clock buffer
• Eliminate skew between clock input and internal clock-input pins within the device
• Each can drive two global clock networks
• Clock edges reach internal flip-flops 1 to 4 clock periods after they arrive at the input.
• Provides control of multiple clock domains (See Tables 1 and Figures 4 & 7 for DLL app note XAPP132)
• Has minimum clock frequency restrictions!
Boundary Scan

- IEEE(ANSI) Standard 1149.1
- Provides Ability to Observe and Control I/Os
- Accessed Through a Standard Test Access Port (TAP)
- TAP Has Four Inputs (TCK, TMS, TDI) and One Output (TDO)
- Additional Logic Includes Test Instruction Register, ID Register, two User Registers and a One Bit Bypass Register.
- Uses:
  - Test Interconnects between ICs on Boards
  - Perform Tests on Internal Logic
  - Initial Built-In Self-Test Logic
  - Perform Sampling During Normal Operation
- See Figure 10: Virtex Series Boundary Scan Logic
Configuration - How Is It Implemented?

- Implemented by loading configuration data into 2-D configuration SRAM
- See Table 7: Configuration Modes
  - Mode selected by Mode Pins - Dedicated pins, M0, M1, and M2 for configuration
- See Table 11: Virtex Bit Stream Lengths
Tables 7 & 11: Configuration Modes & Bit Stream Lengths

<table>
<thead>
<tr>
<th>Configuration Mode</th>
<th>M2</th>
<th>M1</th>
<th>M0</th>
<th>CCLK Direction</th>
<th>Data Width</th>
<th>Serial D_out</th>
<th>Configuration Pull-ups</th>
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<td>Master-serial mode</td>
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</table>

<table>
<thead>
<tr>
<th>Device</th>
<th># of Configuration Bits</th>
</tr>
</thead>
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<tr>
<td>XCV50</td>
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<tr>
<td>XCV1000</td>
<td>6,127,744</td>
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</tbody>
</table>

Summary of XCV800 Characteristics

- Maximum Gate Count: 888,439
- CLB Matrix: 56 x 84
- Logic Cells: 21,168
- Maximum IOBs: 512
- Flip-Flop Count: 43,872
- Block RAM Bits: 114,688
- Horizontal TBUF Long Lines: 224
- TBUFS per Long Line: 168
- Program Data (bits): 4,715,616
Summary of XCV800 Characteristics (continued)

- Interconnections
  - Single Length 24
  - Hex Length 72
  - Longlines 12
  - Globals - Primary 4
  - Globals - Secondary (Backbone) 24
  - Carry Logic 2

References

- On-Line Xilinx Data Sheet DS003 (v.2.5, April 2, 2001)
- XAPP130 Using the Virtex Block SelectRAM+ Features (v1.4)
- XAPP132 Using the Virtex Delay-Locked Loop (v2.6)