

ECE 554 COUNTDOWN

● DEMONSTRATION

- ◆ Scheduling
- ◆ Miscellaneous
- ◆ Content

● FINAL REPORT

- ◆ Check-In
- ◆ Content

● FEEDBACK

04/30/2003

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DEMONSTRATION - Scheduling

- Available Times
 - ◆ Monday, May 5 or Wednesday, May 7 - 3:30 - 5:00 PM or 5:00 PM - 6:30 PM (Actual session length may be as long as 2 hrs)
 - ◆ Tuesday, May 6 or Thursday, May 8 - 3:45-5:15 PM or 5:15 PM - 6:45 PM (Actual session length may be as long as 2 hrs)
- Teams have priority during their normal lab periods
- The team leader is to request a demonstration time at least 24 hours in advance, preferably sooner
- The request must include:
 - ◆ the time requested plus an alternate time
 - ◆ a team name
 - ◆ a project name, and
 - ◆ a project description between 150 and 250 words to be distributed with an announcement of the demonstration and posted on the course website
- The demo time will be selected on a first-come, first serve basis within the above constraints and will be confirmed by e-mail to the class plus others.

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DEMONSTRATION - Miscellaneous

- In the event of last minute problems, a demo can be delayed up to two hours, but must yield to a following scheduled demo
- Attendance of Members of Team Doing Demo Required
 - ◆ Other teams invited to attend
 - ◆ Other guests welcome.
- LCD Projector and Laptop Available

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DEMONSTRATION - Content

- 20 Minutes System Overview
 - ◆ Basic Characteristics
 - ◆ Stress main theme/features
 - ◆ Any presentation on software should be high-level.
 - 20 Minute System Demonstration
 - ◆ Instruction set exercise; software which demonstrates system features
 - 20 Minutes Questions
 - ◆ Empirical evaluation of clock rate (if feasible)
 - ◆ Performance-enhancing features
 - ◆ FPGA Utilization
 - 10 Minutes for Photos
 - 10 Minutes for Instant Feedback
- * See *Demonstration* section in Project part of Lab Manual.

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FINAL REPORT - Check-in

- TWO copies due NOON, Wednesday, May 14 – 3441 Engineering Hall
- Self - contained & one copy non-returnable
- Return of ALL keys checked out to team members

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FINAL REPORT - Content

- Principles of Operation
- Architecture
- Detailed Design of Each Subsystem (Diagrams/Verilog - Well-Commented; Explanations of Operation)
- Annotated Software Printouts
- Clocking, FPGA Utilization and Speed Information
- Team Consensus Reports on Individual Contributions including % contributions to various project tasks

* See *Final Report* section in Project writeup

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FEEDBACK

- We will attempt to do a brief evaluation of your project at the end of the demo
- Request your letter grade be sent to you by e-mail by mailing kime@engr.wisc.edu before Friday, May 16
- You may get individual feedback on the overall project at a later time from the course instructor
- You may borrow the archived team report we keep for copying; there will be few if any marks on it.

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