ECE556 Design Automation for Digital Systems

Final Project

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A Timing-Driven Global Router

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Introduction:

As the increase of the chip size, more and more gates and other circuits can be fitted into a single chip. The consideration of interconnection capacitance and resistance become essential and can not be ignored. This is because the time constant is the product of the resistance that drives the output and the total load capacitance. When the connections become longer and longer, more and more resistance and capacitance will contribute to the total delay from source to the sink element. As the purpose of optimizing the performance of the chip is concerned, it is critical to estimate the interconnection delay and include into the process of global routing.

Most of the work has been done in global routing does not take the interconnection into account. Instead, the wire length was the only parameter that has been optimized. One question might be asked while reading those papers is: Does the shortest net always gives the shortest wire delay? The answer is ‘NO’. The shortest net will only represent to shortest delay if and only if the wiring resistance is being ignored, which can not be the case nowadays.

The paper that I chose to reference from (see reference 1) was focus on minimizing the interconnection delay as its priority. It uses the delay model presented in another reference paper (reference 2) to do the estimation of delay and represented in part one and the A* path searching algorithm along with the tree structure to as the problem representation and searching tool in part two. In my realization of this paper, however, I have found the fact that it is impossible to write an A* search algorithm in C in a short time; therefore, I used the grid based routing technique that suggested in the class lecture and exhausted searching method.

Method & Algorithm

Delay model representation

The first method that came to mind is the delay approximation, and it is the core of the whole implementation. There are many delay models that people are using to calculate the signal propagation delay in the circuit. There are T models, L models, and \( \pi \) model. The interconnection delay is modeled by using L model as shown in figure two the circuit it approximates is shown in figure one. The two figures can be interpreted as a voltage source having a on-resistance \( R_s \), a wiring resistance \( R \) and wiring capacitance \( C \) and the total load capacitance \( C_L \). The total delay from source \( V_s \) to sink \( C_L \) can be approximated by using the following equation:

\[
D(t) = \beta R_s (C+C_L) + \alpha RC + \beta R C_L
\]  

(1)
In equation (1), $D(t)$ represents the delay from S to t. $R$, and $C$ represent the total resistance and capacitance due to the interconnection. $C_L$ is the total load resistance. The two coefficients $\beta$ and $\alpha$ are found to be 2.21 and 1.02 respectively in calculating the raising time of the signal. With $\beta = 2.21$ and $\alpha = 1.02$, the resultant $D(t)$ is the time needed for signal to reach the 90% of its final value.
Routing region representation

Grid graph is employed to represent the routing region. In the grid representation, vertices model global cells and edges adjacencies between these cells. In this project two layer routing is concerned. For two-layer routing each edge is assigned two numbers to indicate the number of available horizontal and vertical tracks. The following figures explain the routing region.

![Routing Region Diagram](image)

FIGURE 3: The representation of routing region.

In the next section, the programming structure that used to realize the vertices and edges will be announced.

Routs searching method

In the reference paper, it takes the advantage of A* searching technique; however, it is found (as mentioned in the introduction section) to be impossible to have the A* searching done by C programming in the given time; therefore, the exhausted searching method is used instead. The motivation in the exhausted searching is pretty simple. Search through all the possible routs in between the source and sink, and find the best solution, in this project would be the shortest delay. Later in the next section, the program highlight will point out searching algorithm.

Program structure and highlight

The information of each cell was saved in the structure as the shown below:

```c
struct source
{
  int id;  //source node id
  int x;   //x coordinates
}````
int y; //y coordinates
int r; //source output resistance
};

struct sink
{
    int id; //sink node id
    int x; //x coordinates
    int y; //y coordinates
    int c; //Lumped sink capacitance
};

struct edge
{
    int type; //1 = vertical, 2 = horizontal
    int x; //x coordinates
    int y; //y coordinates
    int unit_r; //resistance per unit length
    int unit_c; //capacitance per unit length
    int empty; //occupied or not
    struct edge* nextedge; //pointer to next edge
};

All the information needed for routing and delay calculation all stored in the cell structs, as well as the edge information. The program takes the information and form a link list to perform the routing. After the routing is done, the program will check the delay calculated by a function call ‘cost’ and compare with the best delay recorded. The program will also check the routing is legal or not based on the edge information.
The program is implemented in a way that user can set the different resistance and capacitance according to the different region of the routing space; however, this has to be done manually in the code itself.

Exhausted searching is done by moving two edges at a time, until completely go through all the possible routs from source to sink.

**Results (Performance, code size):**

The total size of the source code is 945 lines. The following is a short example which compared with the router that only take the wire length into account, and another output example with large output file is attached at the end of this report. In the following result, it shows the router that implemented in this project performs better interns of the delay, and it is also maintaining the shortest net length. The initial routing represents the delay when only considers the wire length. Please note that the unit of time is just “time unit”. Since the first three cases the routing went through the same capacitance and resistance; therefore, there is no difference in the resulting delay. **In the last case it shows the improvement in the delay by using this Timing-Driven router.**

The initial routing from source(2, 3) to sink(4, 2) is:

(2, 3) (3, 3) (4, 3) (4, 2)

The estimated delay from the given capacitances and resistances is 2.439500E+02

The final routing from source(2, 3) to sink(4, 2) is:

(2, 3) (2, 2) (3, 2) (4, 2)

The calculated delay from the given capacitances and resistances is 2.439500E+02

The initial routing from source(2, 3) to sink(6, 5) is:

(2, 3) (3, 3) (4, 3) (5, 3) (6, 3) (6, 4) (6, 5)

The estimated delay from the given capacitances and resistances is 4.295900E+02

The final routing from source(2, 3) to sink(6, 5) is:

(2, 3) (3, 3) (4, 3) (5, 3) (5, 4) (6, 4) (6, 5)
The calculated delay from the given capacitances and resistances is $4.295900E+02$.

The initial routing from source(2, 3) to sink(3, 6) is:

(2, 3) (3, 3) (3, 4) (3, 5) (3, 6)

The estimated delay from the given capacitances and resistances is $3.119500E+02$.

The final routing from source(2, 3) to sink(3, 6) is:

(2, 3) (2, 4) (2, 5) (2, 6) (3, 6)

The calculated delay from the given capacitances and resistances is $2.748900E+02$.

Another feature in this program is: When the input edge unit capacitance and unit resistance are all equal amount all the edges, it will guarantee to find the shortest routing between the two points.

**Discussion:**

Although the program has many features and when I implemented the program, I tried to take into account as many factors as possible to make the result optimized but most of the parameters are not friendly used. Most of them needed to be manually enter in the code. This is something that can be improved in the future. The result sometimes is not very good, because of the searching method I chose was not the best searching method in the global routing. Other methods are purposed such as A* searching or linear programming will definitely give the better result. The grid based routing space does not well represent the general global routing space either, but for the simplistic reason, I chose grid based instead more complicated ones such as tree.

Stuff that I have learned from this project is the fact that many problems seem easy to solve but yet it could be NP hard or NP complete problem. The topic I have chosen is a NP complete problem, and only the good programming technique can approach the optimal solution. Through out the programming, I have learned more programming skills and am able to think more carefully. A small detail can make a huge difference in the result, especially in programming to solve problems in this course.
The result of a large file:
The improvement is highlighted. For those nets that didn’t improve the delay were because they went through the nets that have the same capacitance and resistance regions.

The initial routing from source(50, 50) to sink(4, 2) is:

(50, 50) (49, 50) (48, 50) (47, 50) (46, 50) (45, 50) (44, 50) (43, 50) (42, 50) (41, 50) (40, 50) (39, 50) (38, 50) (37, 50) (36, 50) (35, 50) (34, 50) (33, 50) (32, 50) (31, 50) (30, 50) (29, 50) (28, 50) (27, 50) (26, 50) (25, 50) (24, 50) (23, 50) (22, 50) (21, 50) (20, 50) (19, 50) (18, 50) (17, 50) (16, 50) (15, 50) (14, 50) (13, 50) (12, 50) (11, 50) (10, 50) (9, 50) (8, 50) (7, 50) (6, 50) (5, 50) (4, 50) (3, 50) (2, 50) (1, 50) (0, 50) (-1, 50) (-2, 50) (-3, 50) (-4, 50) (-5, 50)

The estimated delay from the given capacitances and resistances is 8.549912E+04

The final routing from source(50, 50) to sink(4, 2) is:

(50, 50) (48, 50) (46, 50) (44, 50) (42, 50) (40, 50) (38, 50) (36, 50) (34, 50) (32, 50) (30, 50) (28, 50) (26, 50) (24, 50) (22, 50) (20, 50) (18, 50) (16, 50) (14, 50) (12, 50) (10, 50) (8, 50) (6, 50) (4, 50) (2, 50) (0, 50) (-2, 50) (-4, 50) (-6, 50) (-8, 50) (-10, 50) (-12, 50) (-14, 50) (-16, 50)

The estimated delay from the given capacitances and resistances is 8.549912E+04

The initial routing from source(50, 50) to sink(6, 5) is:

(50, 50) (49, 50) (48, 50) (47, 50) (46, 50) (45, 50) (44, 50) (43, 50) (42, 50) (41, 50) (40, 50) (39, 50) (38, 50) (37, 50) (36, 50) (35, 50) (34, 50) (33, 50) (32, 50) (31, 50) (30, 50) (29, 50) (28, 50) (27, 50) (26, 50) (25, 50) (24, 50) (23, 50) (22, 50) (21, 50) (20, 50) (19, 50) (18, 50) (17, 50) (16, 50) (15, 50) (14, 50) (13, 50) (12, 50) (11, 50) (10, 50) (9, 50) (8, 50) (7, 50) (6, 50) (5, 50) (4, 50) (3, 50) (2, 50) (1, 50) (0, 50) (-1, 50) (-2, 50) (-3, 50) (-4, 50) (-5, 50)

The estimated delay from the given capacitances and resistances is 7.626625E+04

The final routing from source(50, 50) to sink(6, 5) is:

(50, 50) (48, 50) (46, 50) (44, 50) (42, 50) (40, 50) (38, 50) (36, 50) (34, 50) (32, 50) (30, 50) (28, 50) (26, 50) (24, 50) (22, 50) (20, 50) (18, 50) (16, 50) (14, 50) (12, 50) (10, 50) (8, 50) (6, 50) (4, 50) (2, 50) (0, 50) (-2, 50) (-4, 50) (-6, 50) (-8, 50) (-10, 50) (-12, 50) (-14, 50) (-16, 50)
The estimated delay from the given capacitances and resistances is $7.626625 \times 10^4$.

The initial routing from source $(50, 50)$ to sink $(3, 6)$ is:


The estimated delay from the given capacitances and resistances is $8.087937 \times 10^4$.

The final routing from source $(50, 50)$ to sink $(3, 6)$ is:

$(50, 50)$ (48, 49) (46, 48) (44, 47) (42, 46) (40, 45) (38, 44) (36, 43) (34, 42) (32, 41) (30, 40) (28, 39) (26, 38) (24, 37) (22, 36) (20, 35) (18, 34) (16, 33) (14, 32) (12, 31) (10, 30) (8, 29) (6, 28) (4, 27) (2, 26) (0, 25) (-2, 24) (-4, 23) (-6, 22) (-8, 21) (-10, 20) (-12, 19) (-14, 18) (-16, 17) (-18, 16) (-20, 15) (-22, 14) (-24, 13) (-26, 12) (-28, 11) (-30, 10) (-32, 9) (-34, 8) (-36, 7) (-38, 6) (-40, 6) (-42, 6) (-44, 6) (-46, 6) (-48, 6) (-50, 6) (-52, 6) (-54, 6) (-56, 6) (-58, 6) (-60, 6) (-62, 6) (-64, 6) (-66, 6) (-68, 6) (-70, 6) (-72, 6) (-74, 6) (-76, 6) (-78, 6) (-80, 6) (-82, 6) (-84, 6) (-86, 6) (-88, 6) (-90, 6) (-92, 6) (-94, 6) (-96, 6) (-98, 6) (-100, 6) (-102, 6) (-104, 6) (-106, 6) (-108, 6) (-110, 6) (-112, 6) (-114, 6) (-116, 6) (-118, 6) (-120, 6) (-122, 6) (-124, 6) (-126, 6) (-128, 6) (-130, 6) (-132, 6) (-134, 6) (-136, 6) (-138, 6) (-140, 6) (-142, 6) (-144, 6) (-146, 6) (-148, 6) (-150, 6) (-152, 6) (-154, 6) (-156, 6) (-158, 6) (-160, 6) (-162, 6) (-164, 6) (-166, 6) (-168, 6) (-170, 6) (-172, 6) (-174, 6) (-176, 6) (-178, 6) (-180, 6) (-182, 6) (-184, 6) (-186, 6) (-188, 6) (-190, 6) (-192, 6) (-194, 6) (-196, 6) (-198, 6) (-200, 6) (-202, 6) (-204, 6) (-206, 6) (-208, 6) (-210, 6) (-212, 6) (-214, 6) (-216, 6) (-218, 6) (-220, 6) (-222, 6) (-224, 6) (-226, 6) (-228, 6) (-230, 6) (-232, 6) (-234, 6) (-236, 6) (-238, 6) (-240, 6) (-242, 6) (-244, 6) (-246, 6) (-248, 6) (-250, 6)

The estimated delay from the given capacitances and resistances is $8.087937 \times 10^4$.

The initial routing from source $(50, 50)$ to sink $(9, 9)$ is:

$(50, 50)$ (49, 50) (48, 50) (47, 50) (46, 50) (45, 50) (44, 50) (43, 50) (42, 50) (41, 50) (40, 50) (39, 50) (38, 50) (37, 50) (36, 50) (35, 50) (34, 50) (33, 50) (32, 50) (31, 50) (30, 50) (29, 50) (28, 50) (27, 50) (26, 50) (25, 50) (24, 50) (23, 50) (22, 50) (21, 50) (20, 50) (19, 50) (18, 50) (17, 50) (16, 50) (15, 50) (14, 50) (13, 50) (12, 50) (11, 50) (10, 50) (9, 50) (8, 49) (7, 48) (6, 47) (5, 46) (4, 45) (3, 44) (2, 43) (1, 42) (0, 41) (-1, 40) (-2, 39) (-3, 38) (-4, 37) (-5, 36) (-6, 35) (-7, 34) (-8, 33) (-9, 32) (-10, 31) (-11, 30) (-12, 29) (-13, 28) (-14, 27) (-15, 26) (-16, 25) (-17, 24) (-18, 23) (-19, 22) (-20, 21) (-21, 20) (-22, 19) (-23, 18) (-24, 17) (-25, 16) (-26, 15) (-27, 14) (-28, 13) (-29, 12) (-30, 11) (-31, 10) (-32, 9) (-33, 8) (-34, 7) (-35, 6) (-36, 5) (-37, 4) (-38, 3) (-39, 2) (-40, 1)

The estimated delay from the given capacitances and resistances is $6.555404 \times 10^4$. 
The final routing from source(50, 50) to sink(9, 9) is:

(50, 50) (48, 49) (46, 48) (44, 47) (42, 46) (40, 45) (38, 44) (36, 43) (34, 42) (32, 41) (30, 40) (28, 39) (26, 38) (24, 37) (22, 36) (20, 35) (18, 34) (16, 33) (14, 32) (12, 31) (10, 30) (8, 29) (6, 28) (4, 27) (2, 26) (0, 25) (-2, 24) (-4, 23) (-6, 22) (-8, 21) (-10, 20) (-12, 19) (-14, 18) (-16, 17) (-18, 16) (-20, 15) (-22, 14) (-24, 13) (-26, 12) (-28, 11) (-30, 10) (-32, 9) (-31, 9) (-30, 9) (-29, 9) (-28, 9) (-27, 9) (-26, 9) (-25, 9) (-24, 9) (-23, 9) (-22, 9) (-21, 9) (-20, 9) (-19, 9) (-18, 9) (-17, 9) (-16, 9) (-15, 9) (-14, 9) (-13, 9) (-12, 9) (-11, 9) (-10, 9) (-9, 9) (-8, 9) (-7, 9) (-6, 9) (-5, 9) (-4, 9) (-3, 9) (-2, 9) (-1, 9) (0, 9) (1, 9) (2, 9) (3, 9) (4, 9) (5, 9) (6, 9) (7, 9) (8, 9) (9, 9)

The estimated delay from the given capacitances and resistances is 6.555404E+04

The initial routing from source(50, 50) to sink(11, 12) is:


The estimated delay from the given capacitances and resistances is 5.854545E+04

The final routing from source(50, 50) to sink(11, 12) is:

(50, 50) (48, 49) (46, 48) (44, 47) (42, 46) (40, 45) (38, 44) (36, 43) (34, 42) (32, 41) (30, 40) (28, 39) (26, 38) (24, 37) (22, 36) (20, 35) (18, 34) (16, 33) (14, 32) (12, 31) (10, 30) (8, 29) (6, 28) (4, 27) (2, 26) (0, 25) (-2, 24) (-4, 23) (-6, 22) (-8, 21) (-10, 20) (-12, 19) (-14, 18) (-16, 17) (-18, 16) (-20, 15) (-22, 14) (-24, 13) (-26, 12) (-27, 12) (-26, 12) (-25, 12) (-24, 12) (-23, 12) (-22, 12) (-21, 12) (-20, 12) (-19, 12) (-18, 12) (-17, 12) (-16, 12) (-15, 12) (-14, 12) (-13, 12) (-12, 12) (-11, 12) (-10, 12) (-9, 12) (-8, 12) (-7, 12) (-6, 12) (-5, 12) (-4, 12) (-3, 12) (-2, 12) (-1, 12) (0, 12) (1, 12) (2, 12) (3, 12) (4, 12) (5, 12) (6, 12) (7, 12) (8, 12) (9, 12) (10, 12) (11, 12)

The estimated delay from the given capacitances and resistances is 5.854545E+04

The initial routing from source(50, 50) to sink(20, 22) is:

(50, 50) (49, 50) (48, 50) (47, 50) (46, 50) (45, 50) (44, 50) (43, 50) (42, 50) (41, 50) (40, 50) (39, 50) (38, 50) (37, 50) (36, 50) (35, 50) (34, 50) (33, 50) (32, 50) (31, 50) (30, 50) (29, 50) (28, 50) (27, 50) (26, 50) (25, 50) (24, 50) (23, 50) (22, 50) (21, 50) (20, 50) (19, 50) (18, 49) (17, 48) (16, 47) (15, 46) (14, 45) (13, 44) (12, 43) (11, 42) (10, 41) (9, 40) (8, 39) (7, 38) (6, 37) (5, 36) (4, 35) (3, 34) (2, 33) (1, 32) (0, 31) (1, 30) (2, 29) (3, 28) (4, 27) (5, 26) (6, 25) (7, 24) (8, 23) (9, 22) (10, 21) (11, 20) (12, 19) (13, 18) (14, 17) (15, 16) (16, 15) (17, 14) (18, 13) (19, 12) (20, 11) (21, 10) (22, 9) (23, 8) (24, 7) (25, 6) (26, 5) (27, 4) (28, 3) (29, 2) (30, 1) 20, 21, 22)

The estimated delay from the given capacitances and resistances is 5.843658E+04
The final routing from source(50, 50) to sink(20, 22) is:
(50, 50) (48, 49) (46, 48) (44, 47) (42, 46) (40, 45) (38, 44) (36, 43) (34, 42) (32, 41) (30, 40) (28, 39) (26, 38) (24, 37) (22, 36) (20, 35) (18, 34) (16, 33) (14, 32) (12, 31) (10, 30) (8, 29) (6, 28) (4, 27) (2, 26) (0, 25) (-2, 24) (-4, 23) (-6, 22) (-8, 21) (-10, 20) (-12, 19) (-14, 18) (-16, 17) (-18, 16) (-20, 15) (-22, 14) (-24, 13) (-26, 12) (-27, 12) (-28, 12) (-29, 12) (-28, 12) (-27, 12) (-26, 12) (-25, 12) (-24, 12) (-23, 12) (-22, 12) (-21, 12) (-20, 12) (-19, 12) (-18, 12) (-17, 12) (-16, 12) (-15, 12) (-14, 12) (-13, 12) (-12, 12) (-11, 12) (-10, 12) (-9, 12) (-8, 12) (-7, 12) (-6, 12) (-5, 12) (-4, 12) (-3, 12) (-2, 12) (-1, 12) (0, 12) (1, 12) (2, 12) (3, 12) (4, 12) (5, 12) (6, 12) (7, 12) (8, 12) (9, 12)
The estimated delay from the given capacitances and resistances is 3.438658E+04

The initial routing from source(50, 50) to sink(9, 12) is:
(50, 50) (49, 50) (48, 50) (47, 50) (46, 50) (45, 50) (44, 50) (43, 50) (42, 50) (41, 50) (40, 50) (39, 50) (38, 50) (37, 50) (36, 50) (35, 50) (34, 50) (33, 50) (32, 50) (31, 50) (30, 50) (29, 50) (28, 50) (27, 50) (26, 50) (25, 50) (24, 50) (23, 50) (22, 50) (21, 50) (20, 50) (19, 50) (18, 50) (17, 50) (16, 50) (15, 50) (14, 50) (13, 50) (12, 50) (11, 50) (10, 50) (9, 50) (9, 49) (9, 48) (9, 47) (9, 46) (9, 45) (9, 44) (9, 43) (9, 42) (9, 41) (9, 40) (9, 39) (9, 38) (9, 37) (9, 36) (9, 35) (9, 34) (9, 33) (9, 32) (9, 31) (9, 30) (9, 29) (9, 28) (9, 27) (9, 26) (9, 25) (9, 24) (9, 23) (9, 22) (9, 21) (9, 20) (9, 19) (9, 18) (9, 17) (9, 16) (9, 15) (9, 14) (9, 13) (9, 12)
The estimated delay from the given capacitances and resistances is 6.098087E+04

The final routing from source(50, 50) to sink(9, 12) is:
(50, 50) (48, 49) (46, 48) (44, 47) (42, 46) (40, 45) (38, 44) (36, 43) (34, 42) (32, 41) (30, 40) (28, 39) (26, 38) (24, 37) (22, 36) (20, 35) (18, 34) (16, 33) (14, 32) (12, 31) (10, 30) (8, 29) (6, 28) (4, 27) (2, 26) (0, 25) (-2, 24) (-4, 23) (-6, 22) (-8, 21) (-10, 20) (-12, 19) (-14, 18) (-16, 17) (-18, 16) (-20, 15) (-22, 14) (-24, 13) (-26, 12) (-27, 12) (-28, 12) (-29, 12) (-28, 12) (-27, 12) (-26, 12) (-25, 12) (-24, 12) (-23, 12) (-22, 12) (-21, 12) (-20, 12) (-19, 12) (-18, 12) (-17, 12) (-16, 12) (-15, 12) (-14, 12) (-13, 12) (-12, 12) (-11, 12) (-10, 12) (-9, 12) (-8, 12) (-7, 12) (-6, 12) (-5, 12) (-4, 12) (-3, 12) (-2, 12) (-1, 12) (0, 12) (1, 12) (2, 12) (3, 12) (4, 12) (5, 12) (6, 12) (7, 12) (8, 12) (9, 12)
The estimated delay from the given capacitances and resistances is 6.098087E+04

The initial routing from source(50, 50) to sink(14, 15) is:
(50, 50) (49, 50) (48, 50) (47, 50) (46, 50) (45, 50) (44, 50) (43, 50) (42, 50) (41, 50) (40, 50) (39, 50) (38, 50) (37, 50) (36, 50) (35, 50) (34, 50) (33, 50) (32, 50) (31, 50) (30, 50) (29, 50) (28, 50) (27, 50) (26, 50) (25, 50) (24, 50) (23, 50) (22, 50) (21, 50) (20, 50) (19, 50) (18, 50) (17, 50) (16, 50) (15, 50) (14, 50) (13, 49) (14, 48) (14, 47) (14, 46) (14, 45) (14, 44) (14, 43) (14, 42) (14, 41) (14, 40) (14, 39) (14, 38) (14, 37) (14, 36) (14, 35) (14, 34) (14, 33) (14, 32) (14, 31) (14, 30) (14, 29) (14, 28) (14, 27) (14, 26) (14, 25) (14, 24) (14, 23) (14, 22) (14, 21) (14, 20) (14, 19) (14, 18) (14, 17) (14, 16) (14, 15)
The estimated delay from the given capacitances and resistances is 4.911181E+04

The final routing from source(50, 50) to sink(14, 15) is:
The estimated delay from the given capacitances and resistances is \(4.911181 \times 10^4\).

The initial routing from source(50, 50) to sink(13, 18) is:

The estimated delay from the given capacitances and resistances is \(4.646185 \times 10^4\).

The final routing from source(50, 50) to sink(13, 18) is:

The estimated delay from the given capacitances and resistances is \(4.646185 \times 10^4\).

The initial routing from source(50, 50) to sink(29, 30) is:

The estimated delay from the given capacitances and resistances is \(1.735649 \times 10^4\).

The final routing from source(50, 50) to sink(29, 30) is:

The estimated delay from the given capacitances and resistances is \(1.735649 \times 10^4\).
capacitances and resistances is $1.735649 \times 10^4$

The initial routing from source(50, 50) to sink(30, 40) is:

(50, 50) (49, 50) (48, 50) (47, 50) (46, 50) (45, 50) (44, 50) (43, 50) (42, 50) (41, 50) (40, 50) (39, 50) (38, 50) (37, 50) (36, 50) (35, 50) (34, 50) (33, 50) (32, 50) (31, 50) (30, 50) (30, 49) (30, 48) (30, 47) (30, 46) (30, 45) (30, 44) (30, 43) (30, 42) (30, 41) (30, 40)

The estimated delay from the given capacitances and resistances is $9.886350 \times 10^3$

The final routing from source(50, 50) to sink(30, 40) is:

(50, 50) (48, 49) (46, 48) (44, 47) (42, 46) (40, 45) (38, 44) (36, 43) (34, 42) (32, 41) (30, 40) (29, 40) (28, 40) (27, 40) (26, 40) (25, 40) (24, 40) (23, 40) (22, 40) (21, 40) (20, 40) (19, 40) (18, 40) (17, 40) (16, 40) (15, 40) (14, 40) (13, 40) (12, 40) (11, 40) (10, 40)

The estimated delay from the given capacitances and resistances is $9.886350 \times 10^3$

The initial routing from source(50, 50) to sink(45, 50) is:

(50, 50) (49, 50) (48, 50) (47, 50) (46, 50) (45, 50)

The estimated delay from the given capacitances and resistances is $4.394500 \times 10^2$

The final routing from source(50, 50) to sink(45, 50) is:

(50, 50) (49, 50) (48, 50) (47, 50) (46, 50) (45, 50)

The estimated delay from the given capacitances and resistances is $4.394500 \times 10^2$

The initial routing from source(50, 50) to sink(99, 10) is:


The estimated delay from the given capacitances and resistances is $1.968464 \times 10^4$

The final routing from source(50, 50) to sink(99, 10) is:

(50, 50) (51, 50) (51, 49) (52, 49) (53, 49) (54, 49) (55, 49) (56, 49) (57, 49) (58, 49) (59, 49) (60, 49) (61, 49) (62, 49) (63, 49) (64, 49) (65, 49) (66, 49) (67, 49) (68, 49) (69, 49) (70, 49) (71, 49) (72, 49) (73, 49) (74, 49) (75, 49) (76, 49) (77, 49) (78, 49) (79, 49) (80, 49) (81, 49) (82, 49) (83, 49) (84, 49) (85, 49) (86, 49) (87, 49) (88, 49) (89, 49) (90, 49) (91, 49) (92, 49) (93, 49) (94, 49) (95, 49) (96, 49) (97, 49) (98, 49) (99, 49) (99, 48) (99, 47) (99, 46) (99, 45) (99, 44) (99, 43) (99, 42) (99, 41) (99, 40) (99, 39) (99, 38) (99, 37)
The estimated delay from the given capacitances and resistances is $1.968464E+04$

The initial routing from source(50, 50) to sink(12, 80) is:
(50, 50) (49, 50) (48, 50) (47, 50) (46, 50) (45, 50) (44, 50) (43, 50) (42, 50) (41, 50) (40, 50) (39, 50) (38, 50) (37, 50) (36, 50) (35, 50) (34, 50) (33, 50) (32, 50) (31, 50) (30, 50) (29, 50) (28, 50) (27, 50) (26, 50) (25, 50) (24, 50) (23, 50) (22, 50) (21, 50) (20, 50) (19, 50) (18, 50) (17, 50) (16, 50) (15, 50) (14, 50) (13, 50) (12, 50) (12, 51) (12, 52) (12, 53) (12, 54) (12, 55) (12, 56) (12, 57) (12, 58) (12, 59) (12, 60) (12, 61) (12, 62) (12, 63) (12, 64) (12, 65) (12, 66) (12, 67) (12, 68) (12, 69) (12, 70) (12, 71) (12, 72) (12, 73) (12, 74) (12, 75) (12, 76) (12, 77) (12, 78) (12, 79) (12, 80)

The estimated delay from the given capacitances and resistances is $3.319981E+04$

The final routing from source(50, 50) to sink(12, 80) is:
(50, 50) (48, 51) (46, 52) (44, 53) (42, 54) (40, 55) (38, 56) (36, 57) (34, 58) (32, 59) (30, 60) (28, 61) (26, 62) (24, 63) (22, 64) (20, 65) (18, 66) (16, 67) (14, 68) (12, 69) (10, 70) (8, 71) (6, 72) (4, 73) (2, 74) (0, 75) (-2, 76) (-4, 77) (-6, 78) (-8, 79) (-10, 80) (-12, 80) (-14, 80) (-16, 80) (-18, 80) (-20, 80) (-22, 80) (-24, 80) (-26, 80) (-28, 80) (-30, 80) (-32, 80) (-34, 80) (-36, 80) (-38, 80) (-40, 80)

The estimated delay from the given capacitances and resistances is $2.068033E+04$

The initial routing from source(50, 50) to sink(100, 100) is:
(50, 50) (51, 50) (52, 50) (53, 50) (54, 50) (55, 50) (56, 50) (57, 50) (58, 50) (59, 50) (60, 50) (61, 50) (62, 50) (63, 50) (64, 50) (65, 50) (66, 50) (67, 50) (68, 50) (69, 50) (70, 50) (71, 50) (72, 50) (73, 50) (74, 50) (75, 50) (76, 50) (77, 50) (78, 50) (79, 50) (80, 50) (81, 50) (82, 50) (83, 50) (84, 50) (85, 50) (86, 50) (87, 50) (88, 50) (89, 50) (90, 50) (91, 50) (92, 50) (93, 50) (94, 50) (95, 50) (96, 50) (97, 50) (98, 50) (99, 50) (100, 50) (100, 51) (100, 52) (100, 53) (100, 54) (100, 55) (100, 56) (100, 57) (100, 58) (100, 59) (100, 60) (100, 61) (100, 62) (100, 63) (100, 64) (100, 65) (100, 66) (100, 67) (100, 68) (100, 69) (100, 70) (100, 71) (100, 72) (100, 73) (100, 74) (100, 75) (100, 76) (100, 77) (100, 78) (100, 79) (100, 80) (100, 81) (100, 82) (100, 83) (100, 84) (100, 85) (100, 86) (100, 87) (100, 88) (100, 89) (100, 90) (100, 91) (100, 92) (100, 93) (100, 94) (100, 95) (100, 96) (100, 97) (100, 98) (100, 99) (100, 100)

The estimated delay from the given capacitances and resistances is $9.578905E+04$

The final routing from source(50, 50) to sink(100, 100) is:
(50, 50) (50, 51) (50, 52) (50, 53) (50, 54) (50, 55) (50, 56) (50, 57) (50, 58) (50, 59) (50, 60) (50, 61) (50, 62) (50, 63) (50, 64) (50, 65) (50, 66) (50, 67) (50, 68) (50, 69) (50, 70)
The estimated delay from the given capacitances and resistances is 9.578905E+04

The initial routing from source(50, 50) to sink(24, 33) is:

The estimated delay from the given capacitances and resistances is 1.899155E+04

The final routing from source(50, 50) to sink(24, 33) is:

The estimated delay from the given capacitances and resistances is 1.899155E+04

The initial routing from source(50, 50) to sink(4, 21) is:

The estimated delay from the given capacitances and resistances is 5.463205E+04

The final routing from source(50, 50) to sink(4, 21) is:
The estimated delay from the given capacitances and resistances is 5.463205E+04

The initial routing from source(50, 50) to sink(55, 60) is:
(50, 50) (51, 50) (52, 50) (53, 50) (54, 50) (55, 50) (55, 51) (55, 52) (55, 53) (55, 54) (55, 55) (55, 56) (55, 57) (55, 58) (55, 59) (55, 60)
The estimated delay from the given capacitances and resistances is 3.467150E+03

The initial routing from source(50, 50) to sink(72, 81) is:
(50, 50) (51, 50) (52, 50) (53, 50) (54, 50) (55, 50) (56, 50) (57, 50) (58, 50) (59, 50) (60, 50) (61, 50) (62, 50) (63, 50) (64, 50) (65, 50) (66, 50) (67, 50) (68, 50) (69, 50) (70, 50) (71, 50) (72, 50) (72, 51) (72, 52) (72, 53) (72, 54) (72, 55) (72, 56) (72, 57) (72, 58) (72, 59) (72, 60) (72, 61) (72, 62) (72, 63) (72, 64) (72, 65) (72, 66) (72, 67) (72, 68) (72, 69) (72, 70) (72, 71) (72, 72) (72, 73) (72, 74) (72, 75) (72, 76) (72, 77) (72, 78) (72, 79) (72, 80) (72, 81)
The estimated delay from the given capacitances and resistances is 2.372350E+03

The final routing from source(50, 50) to sink(72, 81) is:
(50, 50) (50, 51) (50, 52) (50, 53) (50, 54) (50, 55) (50, 56) (50, 57) (50, 58) (50, 59) (50, 60) (51, 60) (52, 60) (53, 60) (54, 60) (55, 60)
The estimated delay from the given capacitances and resistances is 3.10721E+04

The final routing from source(50, 50) to sink(72, 81) is:
(50, 50) (50, 51) (50, 52) (50, 53) (50, 54) (50, 55) (50, 56) (50, 57) (50, 58) (50, 59) (50, 60) (50, 61) (50, 62) (50, 63) (50, 64) (50, 65) (50, 66) (50, 67) (50, 68) (50, 69) (50, 70) (50, 71) (50, 72) (50, 73) (50, 74) (50, 75) (50, 76) (50, 77) (50, 78) (50, 79) (50, 80) (50, 81) (51, 81) (52, 81) (53, 81) (54, 81) (55, 81) (56, 81) (57, 81) (58, 81) (59, 81) (60, 81) (61, 81) (62, 81) (63, 81) (64, 81) (65, 81) (66, 81) (67, 81) (68, 81) (69, 81) (70, 81) (71, 81) (72, 81)
The estimated delay from the given capacitances and resistances is 2.495005E+04