Outline

- Microprocessor Technology Trends and Design Issues
- Interconnect delay trends
- Circuit type trends
- Research summary
Microprocessor Design Challenges

➤ High performance (> 500 Mhz)
➤ Low cost (< $100)
➤ Low power consumption (< 10W mobile)
➤ More functionality (KNI MMX)
➤ Shorter time to market (< 18 months)
➤ Satisfies different market segments (server, sub-$1000)
➤ Competition
➤ ....
Tentative Class Schedule

- Technology Trends (1 class)
- Interconnect Modeling and Optimization: (1 week)
  - basic routing: maze-routing
  - wire-sizing, buffer-sizing, buffer-insertion
- Introduction to Verilog (1 week)
- Linear programming and Introduction to C and C++ language (1 week)
- Routing: (2 week)
  - Clock routing (0.6 week)
  - Global and channel routing, Tree routing (1.4 week)
- Timing Analysis (1 week)
  - Delay Characterization, Power Characterization
  - PERL and Latch based timing analysis
- Partitioning and Placement (1.5 week)
- Floorplanning (1 week)
Deal With It!

- Higher clock frequencies
- New processes: 0.18 micron, copper
- Architecture level
  - Superscalar, super-pipeline, out-of-order execution, speculative execution, EPIC, VLIW, ILP, multi-thread
- Circuit level
  - Aggressive dynamic circuits synthesis
  - Sizing, parallel re-powering, logic minimization
- Physical Design
  - Performance-driven place and route, floorplaning
  - Wire-sizing, buffer-sizing, buffer-insertion
Extrapolated Year 1999 Wafer Size
Size of Team Explodes
A look at the increase in speed for Intel microprocessors since 1971. Clock rate (in megahertz) with name of processor.
Process Overview

➢ New process (0.18 um)
  ➢ High aspect ratio
  ➢ Low sheet rho (resistance)
  ➢ Low-ε dielectric (capacitance) (3.55 vs. 4.10)
  ➢ Good Electromigration property
  ➢ 6 metal layers
    ➢ M1 tight pitch for density (X-cap)
    ➢ M2-M3 middle pitch for density & performance (X-cap)
    ➢ M4-M6 high pitch (low resistance) for performance (Inductance)

➢ Future
  ➢ Copper - Less resistance more inductance effect
  ➢ SOI - the M1 coupling strange
0.25 Micron, 5 Layer Technology

Tungsten plugs
0.18 Micron, 6 Layer Technology

IEDM 99
Gate Delay v.s. Scaling

$V_{dd} = 1.3V$

$V_{dd} = 1.5V$

IEDM 99
Interconnect Resistance Grows Super Linearly

Sheet Rho (mohm/sq)

- Al, 0.25um, ref [6]
- Al, 0.18um, this work
- Cu, 0.22um, ref [7]
Interconnect Delay Trend

![Graph showing Interconnect Delay Trend with Technology Generation (micron) on the x-axis and Relative RC Delay on the y-axis.]
**SPEED / PERFORMANCE ISSUE**

*The Technical Problem*

![Graph showing delay versus generation for different materials and configurations.]

- **Gate Delay**
- **Sum of Delays, Al & SiO₂**
- **Sum of Delays, Cu & Low κ**
- **Interconnect Delay, Al & SiO₂**
- **Interconnect Delay, Cu & Low κ**

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**Al**  
**Cu**  
**SiO₂**  
**Low κ**  
**Al & Cu**  
**Al & Cu Line**

- **3.0 μΩ • cm**
- **1.7 μΩ • cm**
- **κ = 4.0**
- **κ = 2.0**
- **.8 μ Thick**
- **43 μ Long**

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*Figure 3: Calculated Gate and Interconnect Delay versus Technology Generation*
Interconnect Complicated Design Flow

Architecture

RTL

Logic

Gate

Layout

Over tens of iterations!
Signal Integrity
A new design challenge
Inductance effect emerging

- An old clock tree
  - Freq domain up to 1Ghz
  - PVL and PRIMA with order 16 find the exact

- A newer ckt, a section of power grid
  - Has L’s
  - PVL and PRIMA with 60th order
  - Frequencies more than 0.6 Ghz are not covered
Some MOR result

- TIM
- Multi-Point PRIMA-34
- PVL-80
- PRIMA-80
In homogeneous, isotropic, linear, time-invariant media,

\[ H' = B \]
\[ \mathbf{E} = \mathbf{B} \]
\[ \text{Ohm's Law} \]
\[ \mathbf{J} = \mathbf{S} \]

Auxiliary medium - dependent equations

\[ \int \nabla \cdot \mathbf{J} = sp \cdot \mathbf{B} - sp \cdot \left( \frac{\mathbf{E}}{\mathbf{B}} \right) \int \mathbf{J} = 1p \cdot \mathbf{B} \]

\[ 0 = sp \cdot \mathbf{B} \]

or

\[ \rho = \sigma \cdot \Delta \]
\[ \mathbf{J} + \frac{\mathbf{E}}{\mathbf{B}} = \mathbf{H} \times \Delta \]

\[ 0 = B \cdot \Delta \]

Interconnected obeys Maxwell's equations
Designs prefer Kirchhoff
We need efficient tools to analyze the interconnect dominant circuits (power grids, packages etc.) accurately in a reasonable amount of time.

⇒ Promising Model Order Reduction (MOR) techniques
Power Consumption

\[ P \sim C V^2 f, \text{ where} \]
\[ C = \text{Capacitance} \sim \text{Area} \]
\[ V = \text{Supply Voltage} \]
\[ f = \text{Operation Frequency} \]
Power Trend
Supply Voltage Trends

![Graph showing supply voltage trends](image)

- $V_{CC}$
- $(V_{CC} - V_T)$
- Gate over drive
- $V_T$

Technology Generation ($\mu$m)
Deal With It!

- **Interconnect**
  - Wire- and Repeater- Sizing
  - Repeater Insertion
  - Performance-driven noise-aware routing
  - **New material:** Low resistance (Cooper), Low k material (SiN2)

- **Gates**
  - Gate Sizing
  - **New Circuit Exploration - Dynamic Circuit, Dual Vt**

- .....

Standby Power Trend

- Active Power
- Pentium II Processor
- 386 CPU
- 486DX

Power (W)

- Standby Power (Transistor T=110°C)

Technology Generation (μm)
Threshold Voltage v.s. Supply Voltage

- Gate drive rule: $V_T < (1/4)V_{CC}$
- Projected .7X scaling

Graph shows $V_{CC}/V_T$ vs. $L_{GATE}$ (μm) with Intel's Technology Trend and projected $0.7X$ scaling.
Vt v.s. Delay

Delay ($\tau_D$) of Static CMOS path

<table>
<thead>
<tr>
<th>$\Delta V_T$ (mV)</th>
<th>% Delay Reduction</th>
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</thead>
<tbody>
<tr>
<td>50</td>
<td>8% 4X</td>
</tr>
<tr>
<td>100</td>
<td>15% 18X</td>
</tr>
<tr>
<td>150</td>
<td>23% 75X</td>
</tr>
</tbody>
</table>

$0.25 \mu m \ V_{CC} = 1.8V$

$\Delta V_T$:
- 50 mV: 8% Delay Reduction
- 100 mV: 15% Delay Reduction
- 150 mV: 23% Delay Reduction

$I_{OFF}$ Increase:
- 4X
- 18X
- 75X
Dual Vt circuit

High Vt

Low Vt
Aggressive circuit styles

PDN

PDN

Static Inverter with Level Restorer
Clock delayed and Self-resetting dynamic circuits

FIGURE 3.4 Self-Timed Single-ended Domino Structures; Clock-Delayed Domino (a); SRCMOS (b).
## Process Limitations

<table>
<thead>
<tr>
<th>FEATURE</th>
<th>LIMIT</th>
<th>REASON</th>
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</thead>
<tbody>
<tr>
<td>Oxide Thickness</td>
<td>2.3 nm</td>
<td>Leakage ($I_{GATE}$)</td>
</tr>
<tr>
<td>Junction Depth</td>
<td>30 nm</td>
<td>Resistance ($R_{SDE}$)</td>
</tr>
<tr>
<td>Channel Doping</td>
<td>$V_T=0.25$ V</td>
<td>Leakage ($I_{OFF}$)</td>
</tr>
<tr>
<td>SDE Under Diffusion</td>
<td>15 nm</td>
<td>Resistance ($R_{INV}$)</td>
</tr>
<tr>
<td>Channel Length</td>
<td>0.06 $\mu$m</td>
<td>Leakage ($I_{OFF}$)</td>
</tr>
<tr>
<td>Gate Length</td>
<td>0.10 $\mu$m</td>
<td>Leakage ($I_{OFF}$)</td>
</tr>
</tbody>
</table>