All Digital Ultra-Fast Acquisition PLL

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2. Introduction

Frequency synthesizers find use in all high frequency applications such as communications, radar, digital communications, electronic imaging and spectroscopy [1]. There are three main techniques commonly used 1) PLL synthesizers based on a feedback mechanism to lock to a reference frequency. The popularity of the PLL is due to their extended tracking range and low cost. 2) Direct analog frequency synthesizers based on a main reference and group of frequencies derived by mixing, filtering, adding, subtracting or dividing as needed. The DA offers excellent spectral purity and fast switching speeds. 3) Direct digital synthesizers use digital techniques to create and modulate a signal that is eventually converted to analog form using a DAC.

3. Motivation

Applications in mm wave radio and Asynchronous Optical Sampling Spectroscopy would benefit from advances in frequency and resolution of a direct digital frequency synthesizer.

Asynchronous Optical Sampling Spectroscopy [1]
In conventional THz-TDR, mechanical delay limits the S/N ratio achieved in a given amount of time. ASOPS uses the time delay between 2 lasers, ramped from 0 to $\frac{1}{f_s}$ at the rate given by Δf_R to eliminate the mechanical delay. Acquisition speed can be improved with high scan rates . Frequency resolution can be improved with better repetition rate stabilization.

Time resolution is given by $S=\frac{\Delta}{f_1 f_2}$, where $\Delta = f_1 - f_2$ and the signal appears expanded in the time axis by a factor $\frac{f_2}{\Delta}$. Thus stability and phase noise in Δ directly affects the accuracy of the time-base.

Advantages of ASOPS

1) High acquisition speed (can capture dynamic events) *speed improves as Δ increases*
2) High spectral resolution resulting from capturing a temporal window the size of the THz pulse period, which would be the theoretical limit. *resolution improves as $\frac{f_2}{\Delta}$ increases*

Thus improvements in $\frac{f_2}{\Delta}$ and $\Delta = f_1 - f_2$ that can be achieved using a DDFS in the laser control loop would greatly benefit ASOPS. A hybrid of a PLL and a DDS based frequency synthesizer could have added benefit.

4. State of the Art

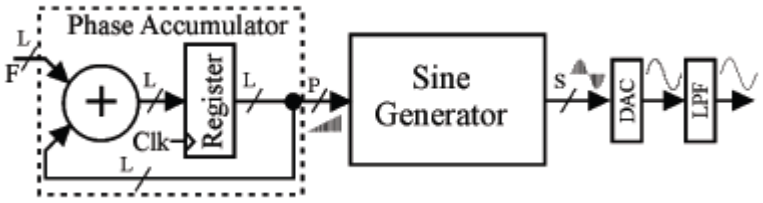

Figure 1 Basic direct digital frequency synthesis

The basic DDFS was proposed by Tierney [2] in 1971 and the main elements are shown below. A summary of the advantages and disadvantages of the various approaches for direct digital frequency synthesis is well summarized in the Ref. [3]. For the phase-to-sinusoid amplitude converter (PSAC) an angular decomposition involves segmenting the phase angles into adjacent bits and expressing the phase angle as the sum of coarse and fine angles. Different ROMs are associated with each group of slices and storage requirements are reduced using trignometric identities. The disadvantage of this method is the approximations resulting from the trignometric identities. Angular rotation based methods have been used to eliminate the ROM LUT. These include the CORDIC (coordinate rotation digital computer) based methods that involve angle rotation. Grayver and Daneshrad [4], pointed out that once the high precision sine and cosine angles are calculated then a recursive calculation can be done to implement a coupled form oscillator. A sine amplitude compression method consists of calculation of a coarse approximation of the sine function and store the residual error in a ROM, the contents of which are added to the approximation. Continuous polynomial approximations can be used for sine amplitude compression. Another method to reduce ROM size is using multipartite table method, which consists of decomposing the LUT into H+1 ROMs and a table of initial values plus H table of offsets (TOs) [7]. The tradeoff is between the ROM size and the adder complexity. In systems that use an analogue output DDFS, the DAC performance is the limiting factor. The PSAC-DAC can be combined and such a combination helps eliminate ROM. The disadvantage of this method is the low spurious free dynamic range [3].

The DDFS methods can be combined with PLL based methods to provide the benefits of DDFS e.g. fast switching speed, high resolution, low power and reliability along with the benefits of a PLL, e.g. wide tracking range and low cost. This combination is of great benefit in ASOPS and radar technologies where a linear chirp (linear ramp in frequency) is required.

The below block diagram Figure 2, depicts this hybrid method. However, the phase detection operation is correlational and generates significant amounts of spurs that require a strong loop filter that degrades the transients and limits switching times. Also the purely analog/RF elements of the charge pump are harder to design in latest CMOS technologies because of poor process characterization and parameter spread.

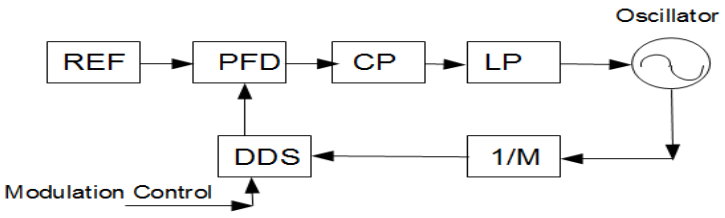

Figure 2 A hybrid PLL and DDS
REF = reference, PFD=Phase/Frequency Detector, CP=Charge pump, LP=Low pass, 1/M= division factor, DDS=Direct digital synthesis

5. Proposed Frequency Synthesizer

The digital PLL chosen for this study is based on the reference from Staszewski [6] and has application in a linear frequency modulated PLL for mm-wave FMCW radars

Introduction
The authors propose a new digitally-intensive frequency synthesizer for a 60 GHz wireless sensing FMCW radar system and verify it though detailed circuit-level and system-level simulations. It consists of a 20 GHz digital PLL and a frequency tripler. The 20 GHz digital PLL features ultra-fast acquisition (less than 5 μs) and low phase noise (-80 dBc/Hz at 100 kHz offset) by adopting dynamic and hitless loop bandwidth control. Linear frequency modulation(LFM) produces a triangle-shaped chirp signal with 3.2 GHz bandwidth in a 2 ms sweep. The maximum frequency deviation is only 0.014% of the chirp bandwidth. A multiplier following the 20 GHz PLL extends the LFM bandwidth to 9.6 GHz centered at 60 GHz, resulting in a range resolution better than 5 cm. The block diagram of the FMCW synthesizer is shown in Figure 3 below

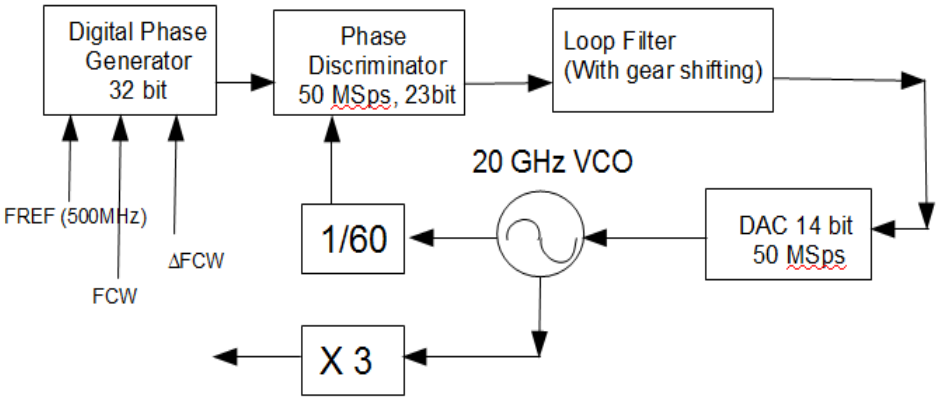

Figure 3 60 GHz FMCW synthesizer

Time domain modeling
The reference and oscillator phases are linear and the difference produced by the phase detector is also linear without any spurs. This is in contrast to the above mentioned charge pump based PLLs, whose phase detection is correlational and generates spurs. Since all the elements other than the VCO are digital, an event driven simulation can be used with many advantages. The main advantage being that only the time instances of interest (e.g. edges) of the clock signals are used to control and synchronize the functionality of the simulated system. Access to time is inherent by adding delays to transitions or by means of time type data objects as in VHDL. Spice based simulation tools are very slow for large circuits since they have to use oversampling which results in excessive data.

This model is based on work from references [8,9,10]

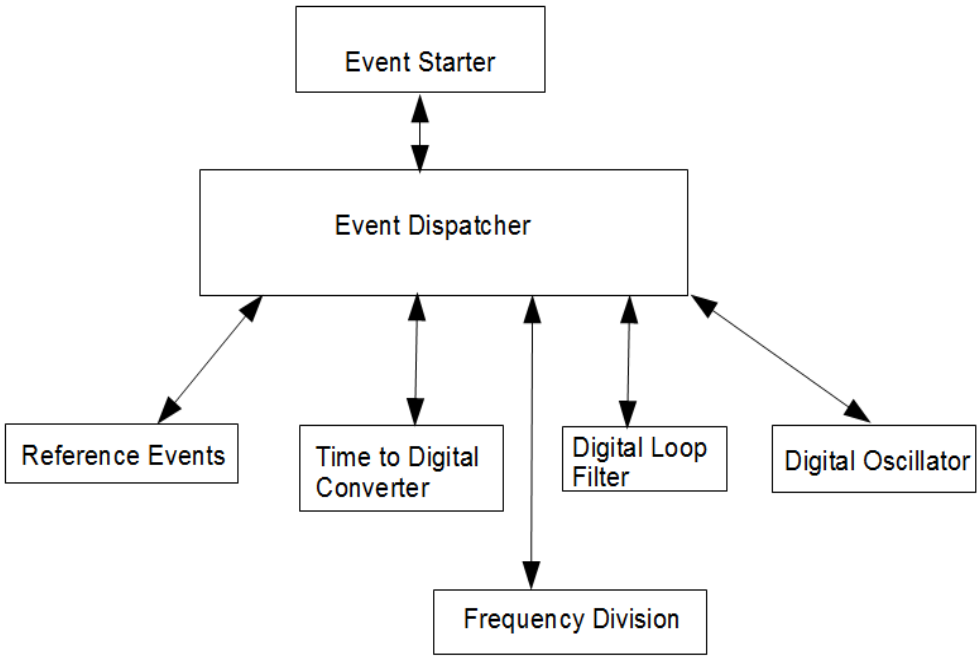

Figure 4: Time domain simulation model of the all-digital PLL

6. Design Parameters

The main design parameters for any PLL are the frequency range, resolution, acquisition speed, phase transient and phase noise. This work focuses on the acquisition speed which is the time to settle within a specific frequency +/- Hz from the target frequency. Commercial handsets for GSM and WCDMA have a acquisition speed of about 150 us. Very low acquisition speeds of 10 us have been achieved but at the expense of larger area and complexity.

The block diagram of the PLL simulated is shown in Figure 5.

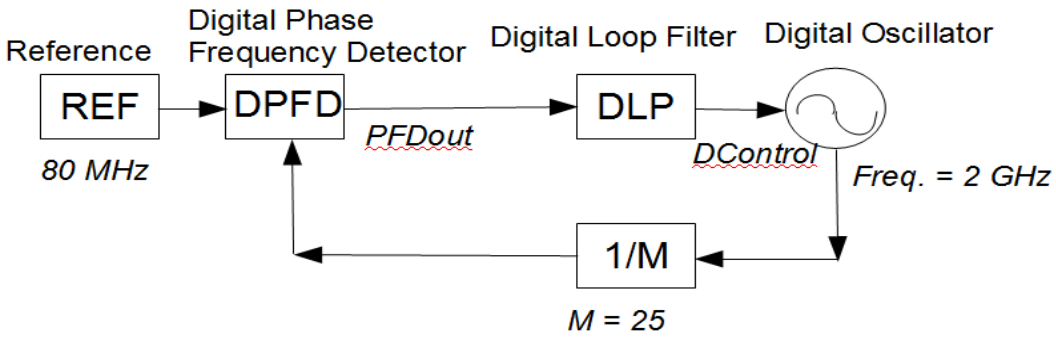

Figure 5: Time domain simulation model of the PLL

The design parameters for the simulation are:

Center frequency:	2 GHz
Frequency range:	+/- 50 MHz around carrier
Frequency step size in digital oscillator:	50 KHz

Main digital variables

PFDout = 2*round(DivTime – RefTime)/100e-12 -1

Thus the maximum value of PFDout is 1250 and requires 12 bits + 1 sign

Dcontrol = round (Int + alpha * IIR)

Maximum value of the integral term is err * $(1 - a^n)/(1-a)$. For the value of a in the design, Dcontrol requires 12 bits + 1 sign bit

Speed-up of the loop filter

A higher bandwidth loop filter would mean a larger chirp bandwidth is possible. Thus it is advantageous to speed-up the loop filter as long as performance is not sacrificed in terms of phase noise and loop stability is maintained.

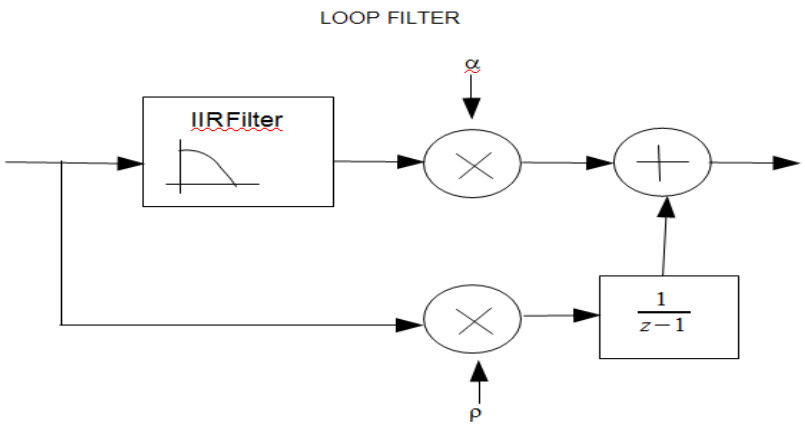

Figure 5 Loop Filter block diagram

The goal of this project is to compare the following loop filters in terms speed while keeping the phase noise unaffected.

1) Baseline case with the IIR block in the above diagram taken as unity.
2) The IIR filter implemented as a type 2 sixth order filter as in Ref [11]. This filter is formed by cascading four single stage IIR filters, each with attenuation factor λ_i where i=0..3. The transfer function of this filter is

$$H_{ol}(s)=\frac{\rho * f_R^2}{s}\,\frac{1+\frac{s}{f_R}}{\frac{\rho}{\alpha}}\,\prod_{i=0}^{i=3}\frac{1+\frac{s}{f_R}}{1+\frac{s}{\lambda_i f_R}}$$

Thus there are two poles at the origin, four poles at $\omega_{p,3+i}=j\lambda_i f_R, for\ i=0..3$

There is one zero at $\omega_{z1}=j(\rho\frac{f_R}{\alpha})$ and four zeros at $\omega_{z,2+i}=j f_R$ for i=0..3

3) Look ahead transformation applicable to recurrent algorithms will be used to reformalate the IIR filter from above. Thus the above cascade of single stage IIR filters can be expressed as a sum of parallel filters. Also any critical paths can be reduced using cut set retiming.

7. Analysis and Simulation Results

Analysis of the Frequency Response of the IIR filters

The bode plot of the loop filters is shown below. This shows a bandwidth of the filters to be in the range of 100 Khz with a phase margin of about 40° for the 4-pole and about 80° for the 2-pole. The 4-pole has a steeper roll-off but at the expense of phase margin.

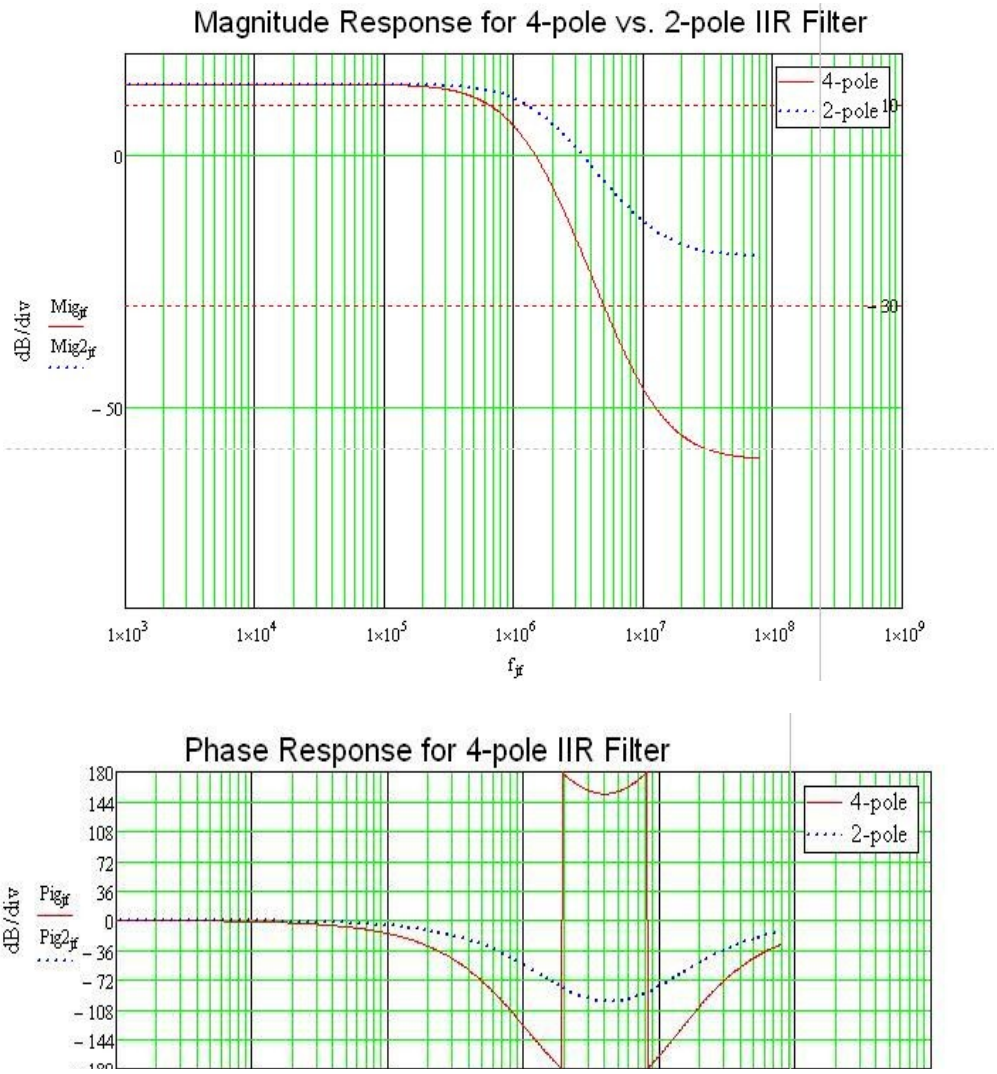

Figure 6 Frequency response of 4-pole and 2-pole IIR filters

Step response of the IIR filter with the integrator in parallel

The closed loop response of the IIR filter with the integrator in parallel is analyzed in MathCAD. The underdamped response is from the addition of the integrator.

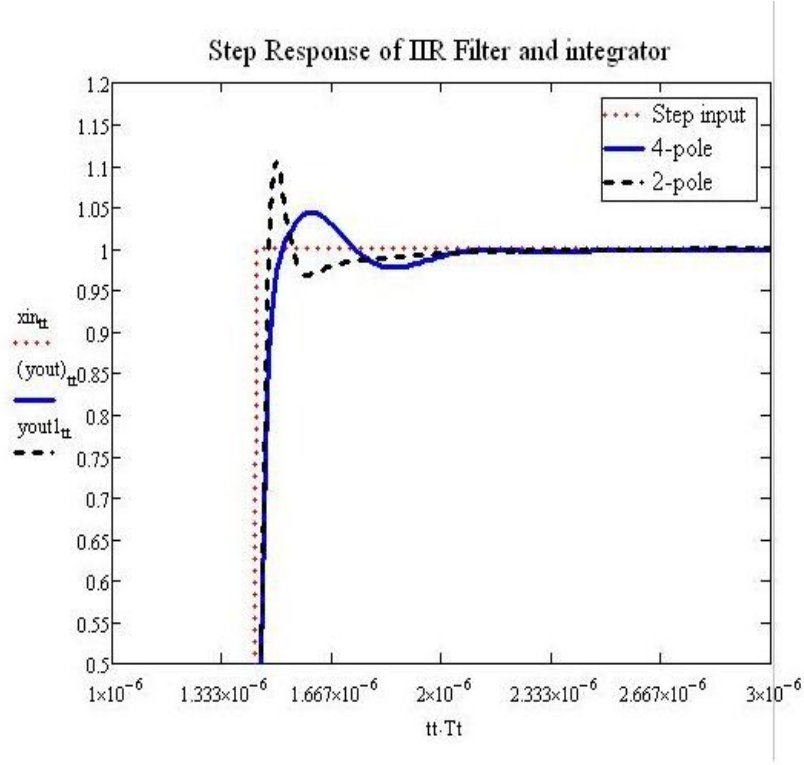

Figure 7 Step response of the 4-pole and 2-pole IIR filters

Simulation Model Verification

The operation of the closed loop PLL controller is verified by observing the error at the output of the time to digital converter. The integrator ensures that the error is centered around zero with the noise observed in the figure resulting from the quantization noise of the converter. As seen from the figure this is between +/-1 counts

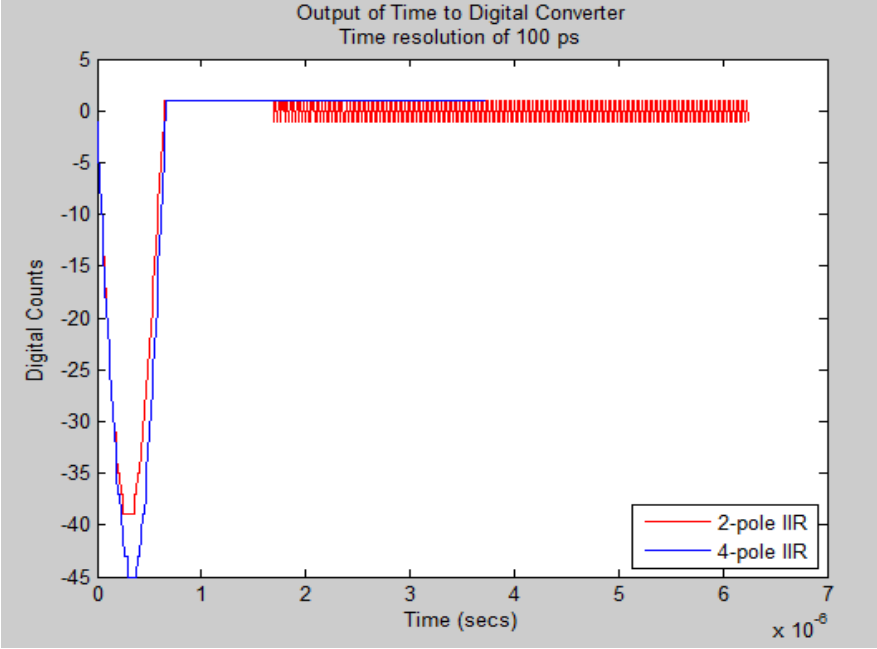

Figure 8 Quantization noise at the time to digital converter

The acquisition time response of the IIR filters is of the order of 1.5 us for a 2-pole filter and about 5 us for the 4-pole filter. This is shown in Figure 9. The response is the fastest without any bandwidth limiting filter as seen by the 0-pole response curve. However, this is not practical as this results in a large quantization noise. This is shown in Figure 10.

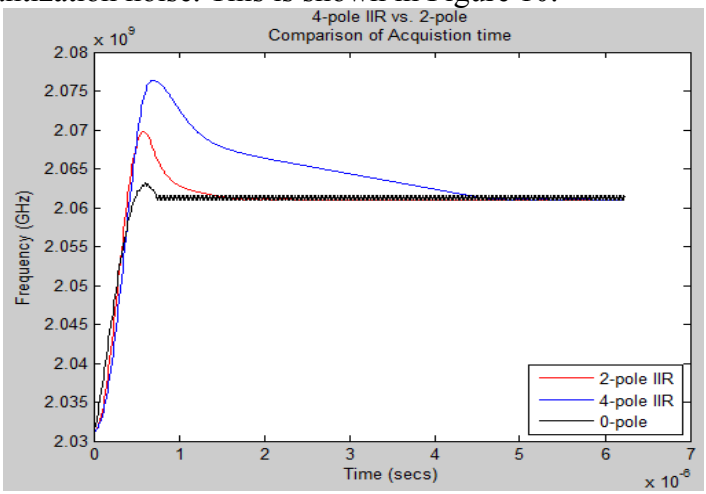

Figure 9 Acquisition time with different filters

The 500 Khz noise as seen without any filter shows the effectiveness of the filters is suppressing the quantization noise.

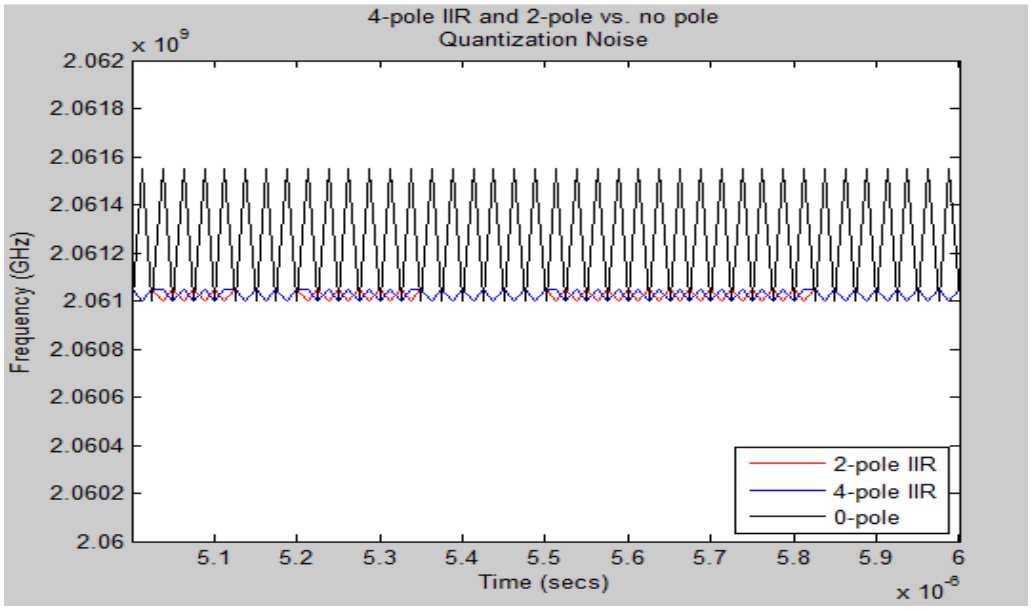

Figure 10 Quantization noise without any filter vs. with filter

Look Ahead transformation with loop unrolling

The IIR filter is a cascade of single pole, single zero stages, with the transfer function of each stage being expressed as:

$y1(k) = (1 - a1) * y1(k-1) + a1 * x(k)$

Substituting once for y1(k-1) transforms the equation to
$y1(k) = (1-a1)^2 y1(k-2) + a1*(1-a1) * x(k-1) + a1 * x(k)$
Thus the iteration bound has been decreased by a factor of two.

Now loop unrolling can be implemented to obtain
$y1(k) = (1-a1)^2 y1(k-2) + a1*(1-a1) * x(k-1) + a1 * x(k)$
$y1(k-1) = (1-a1)^2 y1(k-3) + a1*(1-a1) * x(k-2) + a1 * x(k-1)$
Thus is a serial to parallel conversion and enables parallel execution of independent loops.

The filter is implemented as a cascade of single pole and single zero filters. Thus the second stage equations are written as
$y2(k) = (1-a1)^* y2(k-1) + a1 * y1(k)$
A similar transformation is done for this loop and a 2-pole IIR filter with look ahead transformation and loop unrolling is implemented. The clock frequency of the reference is doubled while keeping the division ratio of the output frequency to the reference the same. Thus a 4 GHz output is obtained. The loop bandwidth is still kept the same by decreasing the integral constant by a factor of two, since the sampling frequency is doubled from 80 MHz to 160 MHz (same as the reference clock frequency). Figure 11 shows that the loop sampling can be increased while keeping performance the same.

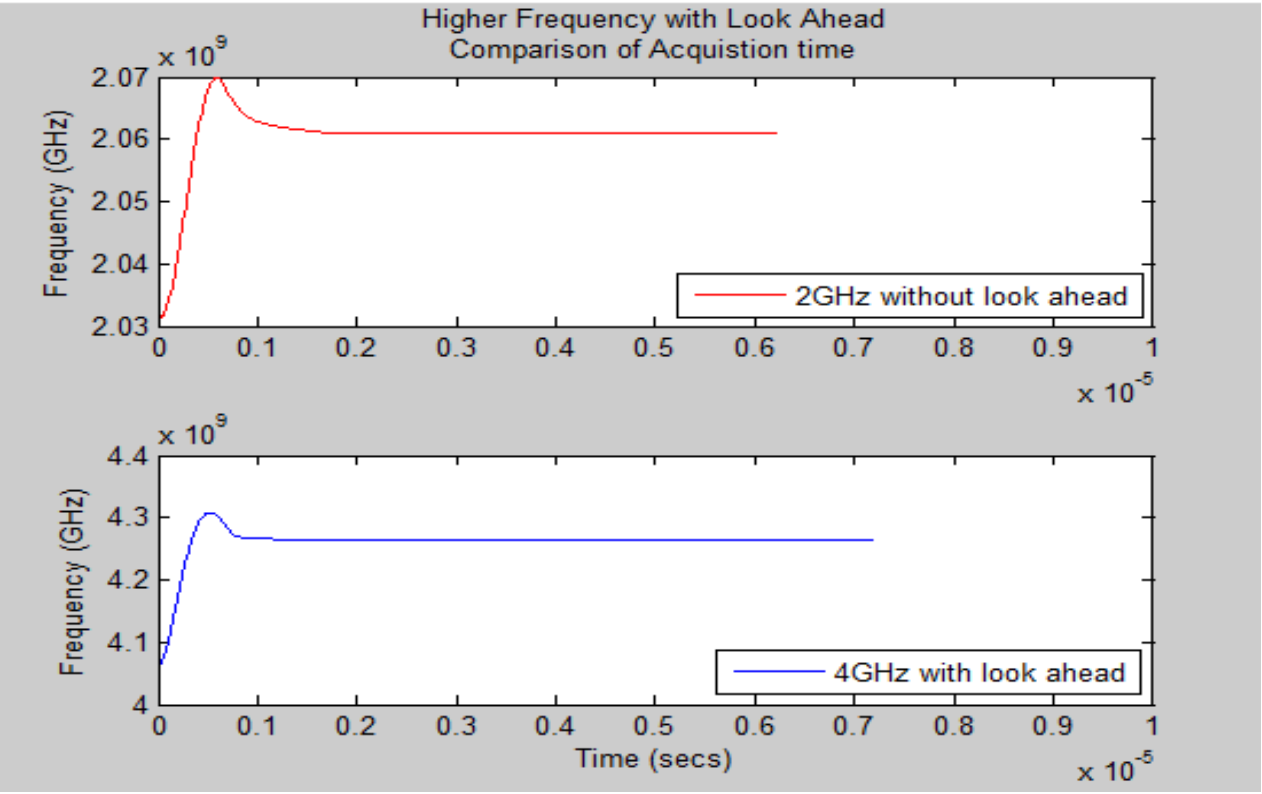

Figure 11 Look ahead transformation enables higher frequency at equal performance

8. Conclusion

This work presents a highly digital frequency synthesizer with application in radars and imaging. A hybrid of a direct digital synthesizer and a PLL is simulated. The analog PLLs with a charge pump generated spurs and hence required a loop filter with a low bandwidth. The time to digital converter does not generate spurs and hence the loop filter bandwidth can be increased without sacrifice of performance. A time domain simulation is used to realize the benefit of speeding up the loop filter in a PLL. An event driven model is implemented in MATLAB. The performance of the PLL is verified and the look ahead transformation along with loop unrolling is used to demonstrate that it is possible to double the clock frequency with a single look ahead transformation. This is done without negatively affecting the performance. Thus this demonstrates that any digital real-time delays in the IIR loop filter can be eliminated with some additional hardware.

References

[1] Markus Brehm, Albert Schliesser, and Fritz Keilmann, 'Spectroscopic near-field microscopy using frequency combs in the mid-infrared', Optics Express, Vol. 14, No. 23,13 November 2006.

[2] Tierney, J., Rader, C.M., and Gold, B., 'A digital frequency synthesizer', IEEE Trans. Audio Electroacoust, 1971, AU-19, pp. 48-57

[3] J.M.P. Langlois and D. Al-Khalili, 'Phase to sinousoid amplitude conversion techniques for direct digital frequency synthesis', IEE Proc.-Circuits Devices Syst., Vol. 151, No. 6, December 2004.

[4] Grayver, E. and Daneshrad, B. 'Direct digital frequency synthesis using a modified CORDIC", Proc. IEEE Int. Symp. On Circuits and Systems, pp. 241-244, 1998.

[5] Byung-Do Yang, Jang-Hong Choi, Seon-Ho Han, Lee-Sup Kim, and Hyun-Kyu Yu, 'An 800-MHz Low-Power Direct Digital FrequencySynthesizer With an On-Chip D/A Converter', IEEE Journal Of Solid-State Circuits, VOL. 39, NO. 5, May 2004

[6] Wanghua Wu, John R. Long and Robert Bogdan Staszewski, 'A Digital Ultra-Fast Acquisition Linear Frequency Modulated PLL for mm-Wave FMCW Radars', 2009 IEEE International Symposium on Radio-Frequency Integration Technology.

[7] Davide De Caro, Nicola Petra, and Antonio G. M. Strollo, 'Reducing Lookup-Table Size in Direct Digital Frequency Synthesizers Using Optimized Multipartite Table Method', IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 55, NO. 7, AUGUST 2008

[8] Robert Bogdan Staszewski and Poras T. Balsara, 'Phase Domain All-Digital Phase-Locked Loop', IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 52, NO. 3, MARCH 2005.

[9] Robert Bogdan Staszewski and Poras T. Balsara, 'Event-Driven Simulation and Modeling of Phase Noise of an RF Oscillator', IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 52, NO. 4, APRIL 2005

[10] Ioannis L. Syllaios, Robert Bogdan Staszewski and Poras T. Balsara, 'Time-Domain Modeling of an RF All-Digital PLL', IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 55, NO. 6, JUNE 2008

[11] Robert Bogdan Staszewski, John Wallberg, Sameh Rezeq, Chih-Ming Hung, Oren E. Eliezer, Sudheer K. Vemulapalli, Chan Fernando, Ken Maggio, Roman Staszewski, Nathan Barton, Meng-Chang Lee, Patrick Cruise, Mitch Entezari, Khurram Muhammad and Dirk Leipold, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL.40, NO.12, DECEMBER 2005.