Implementation of JPEG Encoder for FPGAs using Verilog HDL

Proposal
The JPEG encoder is a major component in JPEG standard which is used in image compression. It involves a complex sub-block discrete cosine transform (DCT), along with other quantization, zigzag and Entropy coding blocks. The aim of the project is the implementation of JPEG encoder for FPGA using efficient utilization of hardware resources. The design process also involves finding techniques to optimize the encoder for maximum performance in FPGA.

Methodology and Time-line
Week1 & 2: The first step of the project will be study of JPEG Encoding techniques. It involves reading of some research papers and online materials on JPEG encoding. The aim is to come to a baseline design for implementation on FPGA keeping in mind the performance and hardware resources used. The first step also requires doing some research on design techniques for FPGA optimization.

Week3 & 4: The next step will be writing the Verilog code for FPGA implementation.

Week5, 6 & 7: The final step involves testing and tuning of design for performance and efficient hardware utilization. The tuning part of the design involves studying the impact on performance due to variations in design parameters. For testing, I will be writing Verilog testbenches to verify the functionality of the encoder. The Verilog code will be synthesized using tool like Quartus.

Motivation
The motivation behind this project is to develop a good understanding of JPEG encoding techniques and its hardware implementation.

References
1. Osman.H “JPEG Encoder for Low-Cost FPGAs “

2. Santosh Sanjeevannavar, Nagamani A.N “Efficient Design and FPGA Implementation of JPEG Encoder using Verilog HDL”