ECE 734 Project Proposal

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Description

The primary objective of the project would be to implement motion estimation algorithm in SystemC/Verilog and optimize the architectural design in the process.

Here is a rough description of the steps involved:

a) **Motion Estimation Research Survey:** From a preliminary search it is clear that research in the topic of motion estimation is very active and different designs have been proposed based on different platforms such as FPGA, SOC's and other implementation suited for VLSI architecture based design. Due to the variety of implementations possible, an investigation of platform dependent optimizations would be required.

b) **Implementing FPGA based design:** The primary goal of the project would be to implement a working implementation of Motion estimation similar to the one proposed in “An FPGA implementation of Motion Estimation Algorithm for H.264/AVC.”[1] This implementation is based on the LDPS (Line Diamond Pattern Search) search algorithm and uses FPGA based memory blocks to have a fast implementation.

c) The primary milestone for the project would be to have a working design by starting with a simpler system requirement like having a fixed block size motion estimator (FSBME) and then develop a variable sized block motion estimator implementation (VSBME).

d) For verifying the correctness of the design results could be compared with a reference software design.

Reason for choosing this topic

The reason for selecting the project proposal is to learn about implementing a critical and computationally intensive block of the H.264 standard like motion estimation. The implementation of motion estimation in hardware makes sense because the general purpose microprocessing doesn't meet the computational requirements for higher frame rates, hence designing and optimizing a motion estimation based accelerator would be really useful topic for general research.

References