Conditioned Reflex Mimic Circuit Design

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Abstract

Neural network holds great promise to be the next generation computer for the sake of its strong capacity of massive parallel processing, good capability of discerning, compatibility with analog computing, self-learning ability, and so on. In this course project, I designed a basic biological function unit cell, which can mimic one basic biological conditioned reflex function in two versions: conventional digital circuit design in Verilog HDL and the version with RRAM (Resistive Random Access Memory) as the synapse in the neuromorphic circuit. The comparison of the two versions shows that the second version with RRAM would have better performance regarding the circuit area, and thus high integrate density, non-volatile memory, bio-competitive power consumption, analog computing compatibility, and stronger circuit learning ability.
1. Introduction

The invention and the popularization of digital computer changed almost every aspect of our life in the passing century. However, the speed of computer engineering’s development cannot always catch up with that of people’s desire. Also microelectronics industry’s fast advance provides many novel devices as well as their fabricating methods. As a result, fast processing, big memory capacity, artificial intelligence are becoming the main trend of this fashion inevitably. Neural computer, with strong capacity of massive parallel processing, good capability of discerning, compatibility with analog computing, and self-learning ability \[^{1-3}\], is becoming one of the strong candidates of the next-generation main-stream computer, which will replace current digital computers.

Many institutes, companies, and universities are currently researching the neuromorphic circuit which can play the role of many neural functions. Most of those researches focus on the image recognition, pattern learning and recall, and parallel computing aiming at high throughput of computation. Few researches concentrate on the biological function simulation, which may supply much for the implementation of the real human-mimic robot which can behave like a man. In this course project, I designed a basic biological function unit cell, which can mimic one basic biological function using RRAM as the synapse of the neural network, which has small area and thus high integrate density, bio-competitive power consumption, analog computing compatibility, and stronger circuit learning ability.

I select Conditioned Reflex to be the target function to be implemented in this project, which was found by the famous Russian physiologist Ivan Pavlov. Many of our human learning processes could be viewed as the process of conditioned reflexes. Thus, it is very important to implement the above function simulating circuit design that can supply one of the basic biological function simulating units for artificial intelligent robot.
2. Background information

2.1 Conditioned Reflex [4]
Classical conditioning (also Pavlovian conditioning or respondent conditioning) is a form of learning in which the conditioned stimulus or CS, comes to signal the occurrence of a second stimulus, the unconditioned stimulus or US. (A stimulus is a factor that causes a response in an organism.) The conditioned response is the learned response to the previously neutral stimulus. [5] The US is usually a biologically significant stimulus such as food or pain that elicits a response from the start; this is called the unconditioned response or UR. The CS usually produces no particular response at first, but after conditioning it elicits the conditioned response or CR.
Conditioning is usually done by pairing the two stimuli, as in Pavlov’s classic experiments. [6] Pavlov presented dogs with a ringing bell followed by food. The food elicited salivation (UR), and after repeated bell-food pairings the bell also caused the dogs to salivate. In this experiment, the unconditioned stimulus is the dog food as it produces an unconditioned response, saliva. The conditioned stimulus is the ringing bell and it produces a conditioned response of the dogs producing saliva.

2.2 RRAM and Memristor

2.2.1 Memristor [7]
The memristor was originally envisioned in 1971 by circuit theorist Leon Chua as a missing non-linear passive two-terminal electrical component relating electric charge and magnetic flux linkage. [8] Leon Chua has said that the memristor definition could be generalized to cover all forms of 2-terminal non-volatile memory devices based on resistance switching effects [9] and Chua has said that the memristor is the oldest known circuit element with its effects predating the resistor, capacitor and inductor. [10] The memristor is currently under development by various teams including Hewlett-Packard, SK Hynix, and HRL Laboratories.
When current flows in one direction through a memristor, the electrical resistance
increases; and when current flows in the opposite direction, the resistance decreases.\textsuperscript{[11]} When the current is stopped, the memristor retains the last resistance that it had, and when the flow of charge starts again, the resistance of the circuit will be what it was when it was last active.\textsuperscript{[12]} The memristor device described by HP is said to have a regime of operation with an approximately linear charge-resistance relationship as long as the time-integral of the current stays within certain bounds.\textsuperscript{[13]}

\textbf{2.2.2 RRAM}

RRAM or ReRAM (Resistive Random Access Memory) is a kind of novel non-volatile memory, which has the advantage of small area and thus high integrate density, simple MIM crossbar structure, non-volatile memory, fast switching speed, low power consumption, compatibility with CMOS process, and simple fabricating process. The above memory, with many other novel memories, is going to be a strong candidate of next generation memory for current flash memory.

The basic idea of RRAM conducting mechanism is that a dielectric, which is normally insulating, can be made to conduct through a filament or conduction path formed after application of a sufficiently high voltage. The conduction path formation can arise from different mechanisms, including defects, metal migration, etc. Once the filament is formed, it may be reset (broken, resulting in high resistance) or set (re-formed, resulting in lower resistance) by an appropriately applied voltage. Recent data suggest that many current paths, rather than a single filament, are probably involved.
Some reports [15-17] also show that RRAM could have multilevel memory ability, which makes the device be a good, even ideal device as the synapse in neuromorphic circuit/system, which requires the synapse device has small area for large scale integration and large memory capability for big learning ability. Also the simple as well as compatible with CMOS fabricating process of RRAM makes it possible for the implementation of neural chip.

3. Circuit design

In this project, I represent the above experiment using the circuits I designed. In general, the experiment could be divided into three phases by the order of time sequence: before learning phase, learning phase, and after learning phase. (1) In the before learning phase, the output of the circuit, which will be used to simulate the process of salivation, will generate value only associated with the food visual input signal but not with the ringing bell sound input signal. (2) In the learning phase, when a bell was rung in subsequent time with food being presented to the dog in consecutive sequences, the dog will initially salivate when the food is presented. The dog will later come to associate the ringing of the bell with the presentation of the food and salivate upon the ringing of the bell. (3) In the after learning phase, the
output of the circuit will generate value associated with both the food visual input signal and the ringing bell sound input signal.

There are two versions of circuit: the first one is the digital circuit design using Verilog HDL, and the second one is a circuit with RRAM as synapse. I will give the detail description of each of those two versions in this part.

3.1 Verilog design

In this part, I first introduce the detail design of my simple version circuit as well as the operating principle of it. And then I give two more versions of circuit which can simulate some more complex functions which fit the real learning process better.

3.1.1 Circuit detail

Here I introduce the verilog design in this part. Below is the circuit block diagram of my digital circuit design version. Using verilog language, we can design the digital circuit easily.

![Fig.2 circuit block diagram of digital circuit design version](image)

From the block diagram we can see the circuit includes two parts: the salivation generate circuit part and the sound weight update circuit part. I will give the detail description for each part below.
In the salivation generate circuit part, the main parts are two weight registers with each 4 bits, two multipliers, and one adder. The food or sound input (4 bits) would give the input signal of food or sound information. Then the input would be multiplied with the corresponding weight value stored in the food_weight or sound_weight register. Finally the weighted input values would be added together and get the salivation output which would be used to generate the salivation. In the following, without specified note, all the values are unsigned value in verilog design,
and for the values, the larger the value is, the stronger the corresponding signal would be.

For the sound weight update circuit part, the value of the most two significant bits of output salivation signal would be the increment of the sound weight and being added into sound weight register. It is ok to use the most two significant bits as the increment of sound weight increment, because it fulfills the biological principle that the more stimulus, the faster the learning speed would be. Also using the most two significant bits as the increment would automatically set a threshold for the sound weight update. That fits biological phenomena that learning would not happen when the stimulus is weak. There is a saturation logic block in the sound weight update circuit shown in fig.3, which is used to make sure the sound weight would never be a wrong value when the updated value is larger than the maximum value that the register could store (the maximum value of 4 bits binary number is 15 in decimal).

### 3.1.2 Operating principle of the designed circuit

At the beginning of our experiment, the initial values of each input and register are shown as following.

food_weight: 4’d15  
sound_weight:4’d0

If an input signal is “0”, that means the corresponding input doesn’t have any input signal. If an input is not “0”, the value stands for the strength of the input. The larger the value is, the stronger the input is. The same definition is also suitable for the output and the registers.
The testing result is given above. After reset, the registers are reset into the value talked above. In the before learning phase, we can see only the food input signal could generate the corresponding salivation output. The sound cannot generate the output even at a high value (4’d15). Then the circuit enters the learning phase when the food and sound inputs are given at the same time. In order to generate large salivation to make the increment of sound weight non-zero, I gave the food input signal 4’d15. We can see in this period, the sound_weight register starts to increase in the way we defined above. And after that, in the after learning phase even without the food signal input, the salivation output would generate value associated with the sound. So this version of circuit works correctly.

3.1.3 Circuit with food weight update
In this part I added food weight update circuit part into the circuit shown in 3.1.1. And the food weight update part and the whole part are shown as below.
The food weight update circuit is the same as the sound weight update circuit except the increment is the most two significant bits of food signal other than the salivation. So using this circuit, we can expect that when the food stimulus is enough strong, the food weight would increase, other than keeping the same value as that in the simple version. Another difference between this circuit version and the former is the initial value of food_weight register is 4’d10.
From the simulating result we can see that in the learning phase the food weight also increase in the way we defined. Other things are same the first simple version circuit.

3.1.4 Circuit with inhibitory mechanism

We note that all the circuits above are only with the excitatory mechanism, because the weights only increase but never decrease. That is not what the actual biological function does. Let’s make the circuit more complex here by adding the inhibitory mechanism. I add a new port which is named by “inhibit”. When the input stays low, the circuit works as the above description. When this input going high, it means the dog gets some bad food which it dislikes, thus the food weight as well as the sound weight would decrease leading to the decrement of salivation. The new circuit is shown below.
food & sound weight update circuit part with inhibitory mechanism

salivation generate circuit part with inhibitory mechanism

Fig. 7 block diagram of food & sound weight update part and the whole salivation generate circuit with inhibitory mechanism
The above testing result shows that when the inhibitory is asserted, the food weight as well as the sound weight would decrease. That is much closer to the reality.

### 3.2 Circuit with RRAM as synapse

Compared with the above circuit versions which use registers being the synapses of the neural network, the circuit using RRAMs as synapses of the neural network has the advantage of small area, low power consumption, multilevel capability and thus stronger learning ability. Besides, the simplicity of processing and compatibility with CMOS also makes RRAM a favor of industry.

Here I designed the conditioned reflex mimic circuit using RRAM as the synapse which is shown as below. In the circuit, M1 and M2 are the food weight synapse and sound weight synapse which are implemented using RRAM, corresponding to the food weight register and sound weight register in the circuit versions above. The input food and sound are the same as food and sound in the above circuit versions. There are two resistances R1 and R2, two inverters inv1 and inv2, two switches S1 and S2. The S1 and S2 switches are closed when the corresponding ctrl voltages are above their threshold. They could be implemented using CMOS switches.
The operating principle of the circuit is as following:

When the food input is high, since at the beginning the food weight connection is strong, which means the M1 resistance is low, the input at inv1 is high, and so the salivation output is high through inv1 and inv2. In the before learning phase the sound weight is weak, which means the M2 resistance is high, so when the food input is low, the voltage at the ctrl1 would not be much high, and thus S1 could not be closed which leads to the salivation output still keep high. In the learning phase, when the food input is high, the voltage at ctrl2 is high leading to the close of S2. The voltage difference across M2 would the sound voltage without any voltage divide by R2. The sound voltage would be larger than the threshold of M2, and then the resistance of M2 would start to decrease which consists of the learning phase. After the learning phase, the resistance of M2 is low, so even when the voltage of food input is low, the input voltage of inv2 would be low to generate the salivation output, since the voltage at ctrl2 is high. The testing result is shown as following.
If we substitute the binary RRAM device with multilevel RRAM device, we can get a network with stronger learning ability but no additional area. We do not need to modify the circuit in order to implement the second version of Verilog design. When the voltage across the M1 surpasses the threshold of M1, the resistance would change. So when the food input voltage is large enough, which means the food is good enough for the dog to generate salivation, the resistance of M1 would decrease leading to stronger connection strength.

We can implement the most complex circuit only by adding three switches. As shown in the figure below, the difference between this circuit and the above one are three additional MOS switches. Here we define that if there is an inhibitory input, the corresponding input voltage should be below than zero. The height of voltage stands for the strength of the stimulus. When there is an inhibitory input from the food input port, once the voltage height is enough high, the current flow through M1 would go in the direction increasing the resistance. At the same time, S3 and S5 would be closed, and S4 would be closed. Then in the learning phase, the only difference from the excitatory input situation is the current flow through M2 is in the direction increasing the resistance of M2 other than decreasing it. Thus the result is the sound weight stored in M2 would decrease when there is an inhibitory food input.
4. Discussion and comparison

Here we will give some discussions about the digital circuit design using Verilog HDL and the circuit using RRAMs as synapses in three aspects: area, non-volatile memory characteristic and power consumption.

Area

Area is one of the most important influence factors of neural network. Because it needs large integrate density of synapses to implement more functions. Here we can do a simple computing of the area of the above versions of circuit. For the complex version of the conditioned reflex mimic circuit using RRAM as synapse, it only needs 9 MOS transistors as well as 2 resistances and 2 RRAM devices. Since the RRAM and resistance could be fabricated in a stackable structure, the total area of that circuit is the area of 9 transistors. However, for 1 bit D flip-flop, as shown in fig.12, it needs 6 NAND gates, each of which includes for MOS transistors. So the total number of transistors of a 1-bit D flip-flop is 24. However, even the simplest digital circuit which only has only 1 bit weight register, would have 68 transistors (multiplier could
be changed by AND gate, and adder could be changed by OR gate. The saturation logic circuit could be deleted in this version). For the circuit with RRAM, if we want the learning ability of the circuit to be stronger, we just need to change the RRAM device by multilevel RRAM device without any area increasing. However, for the digital circuit, if we want the learning ability of the circuit to be stronger, we have to adder more bits to the registers, which would increase much more transistors, and the multipliers, the adders, and the saturation logic would go more complex as the learning ability becoming strong.

![Diagram of a positive edge triggered 1 bit D flip-flop](image)

**Fig.12 a positive edge trigged 1 bit D flip-flop**

**Memory**

The other one advantage of RRAM synapse circuit is the non-volatile characteristic. Since RRAM is a non-volatile device, even when the power is off, the learned information could be saved in the RRAM synapse without any loss. However, for the digital circuit, the register could not keep the learned information in it when power is off. In order to keep the learned information, we have to introduce some other nonvolatile memory system into the circuit, which would definitely increase the complexity, and even the area of the circuit.
**Power consumption**

The other big advantage of RRAM synapse is its low power consumption characteristic with sub-pJ per spike\(^{[18-19]}\) which is biological competitive. The power consumption is a big issue when the circuit scale becomes very large for the integration of more functions. If the power consumption is biological competitive, we do not need to worry much about the power issue of the circuit, which is a very good news for the designer.

5. Conclusion

In this projection, we designed conditioned reflex mimic circuits both using verilog HDL based digital circuit and RRAM synapse based circuit design. Though the two methods could achieve our goal, the second design has many advantages than the first design regarding the circuit area, and high integrate density, non-volatile memory, bio-competitive power consumption, analog computing compatibility, and stronger circuit learning ability.

Reference