1. (15 points) Investigate one of the more recent technology topics; such as biological computing, quantum computing, reversible circuits, carbon-nanotubes, aging phenomenon, soft errors; and identify the problems of interest we may face. In particular the problems that are related to reliability issues and where fault tolerance is likely to offer solutions. Write a one page summary of the problems. Some of you may find this effort leading you to a project of your choice. Submit a printed copy of your report.

Answer:
You can search for information through numerous sources.

2. (10 points) Avizienis in Figure 4 of the paper [aviz:04] lists 16 fault classes. Give an example of each of these classes. You must use a different fault for each class even though a given fault may belong to various different classes.

Answer:

Partial list:

Development faults: Incorrect synthesis, e.g. use of incorrect gate or module type, coding bugs in Software

Operational Faults: HW: aging, SW: incorrect states

Internal faults: HW: short between lines
External faults: Power surge causes device to burn out, SW patch problems

Natural faults: Broken connection

Human Made faults: SW: mistakenly closing a file without saving it.
HW: inserting a wrong IC on a board or wrong board in a system

Hardware fault: Stuck at fault

Software fault: Incorrect coding

Malicious faults: HW: inserting time trigger hardware to activate undesirable logic, SW: virus attacks

Non-malicious faults: HW: opens, SW: system hangs

Deliberate faults: HW: undesirable state encoding, SW: choosing a poor algorithm knowingly

Non-deliberate faults: HW: poor minimization of logic, SW: Writing poor code

Accidental faults: SW: inadvertently overwrite a file, HW: making an incorrect connection between logic gates

Incompetence faults: SW: coding an algorithm without understanding it, HW: designing a circuit without understanding the specifications

Permanent faults: SW: calling a wrong subroutine, HW: a short between a pair of lines

Transient fault: SW: bit flips in the instruction word due to high energy particles, HW: power transients due to occasional excessive power drawn

3. (10 points) Siewiorek in the paper [seiw:95] compares the performance ratio of commercial systems and fault-tolerant systems (refer to Figure 2 in the paper).
It specifies the commercial minis improvement rate of 22.7% and Tandem mini improvement rate of 21.3%. Predict the performance of these (commercial and fault-tolerant systems) systems in the years 2010 and 2020 assuming that commercial systems performed at 10 MIPS in the year 1978 whereas the fault-tolerant systems had that level of performance in 1989. Do you agree with this prediction? Give reason(s) for your answer.

**Answer:**
Improvement rate for commercial system = 22.7%
Improvement for Tandem = 21.3%

Initial condition:

(a) Commercial system in 1978 at 10 MIPS
(b) Tandem in 1989 at 10 MIPS

Hence

(a) Commercial system in 2010 = 10 * (1.227)^{32} = 6966 MIPS
(b) Tandem system in 2010 = 10 * (1.213)^{21} = 577 MIPS
(c) Commercial system in 2020 = 10 * (1.227)^{42} = 53885 MIPS
(d) Tandem system in 2020 = 10 * (1.213)^{31} = 3978 MIPS

Fault tolerant techniques have evolved and are now being used in nearly all commercial systems. With Moore’s law in place - in fact it appears that we are exceeding this goal - largely due to massive hardware redundancy that employs multiprocessing via superscaling, SMT, CMPs etc. Multiple cores on a chip is a norm now and techniques that run a given process or a thread on two or more cores to assure higher reliability are already being used. Large memories that can guarantee the higher performance of all cores are taking place in the sense very often cores have their on L1 and L2 caches to deliver the desired performance.

4. (10 points) Based on the paper by Cristian [cris:91] answer the following:

(a) The term “fault tolerance” has been used ambiguously (p. 77). Explain.

**Answer:**
The paper asserts that it is used to imply the following two conditions,
1. the system has well-defined (specified) failure behavior,
2. the system masks any component failures and performs correctly in the presence of a fault.
(b) Please list the various kinds of failure classification (p. 58).

**Answer:**

The classifications given are:

i. *omission failure* - system omits to respond
ii. *timing or performance failure* - early or late response from a system
iii. *response failure* - an incorrect value or state is delivered
iv. *crash failure* - system omits to outputs for ever till restarted

(c) How a hard (permanent) fault can appear to look like an arbitrary failure at a different level of abstraction.

**Answer:**

An example used in the paper is a clock that fails and displays the same constant time. A communication server which is expected to use a different timestamp for each different message may be construed to have an "arbitrary failure" if it uses such a failed clock value (two different messages will have same timestamps).

(d) What is the distinction between “failure semantic” and ”failure mode” (p.59)?

**Answer:**

Failure semantic will list the behavior of a system for each failure that can occur. In particular for various failure modes the semantic lists operational behavior of the system. The author suggests to use only *failure semantic* and not use alternative terms such as *failure mode*.

(e) What methods have been used to prevent design faults in programs (p. 70)?

**Answer:**

Diverse software design with voting - the author also says that it has generated considerable controversy.

5. (10 points) Breaking FEF chain.

Figure 1 is taken from the book by Johnson [john:89]. This figure does not contain the use of *fault removal* and *fault forecasting*. I believe these two methods can also be used to construct barriers for achieving fault tolerance. Modify this figure (by adding more blocks, more stages, or both) to include fault removal and fault forecasting in this figure. Provide a brief explanation for your answer.
Answer:
It is possible to add these techniques, fault removal and forecasting, at many possible places in the FEF chain. Somewhat more logical choices are at the beginning or at the end of the FEF chain. For example working at board level fault removal can be achieved by thoroughly testing the ICs used in the board thus adding this method at the beginning of the chain. Alternatively testing boards thoroughly puts this method at the end of the FEF chain. Fault forecasting can be similarly used but will typically appear after the fault removal method. Thus one possible fault tolerance methodology is shown in Figure 2

6. (10 points) Fault modeling (HW)
You are provided the following information about a circuit. The technology used is CMOS and the circuit uses only 2 and 3-input NAND gates

# of inputs = 54
# of gates = 350,075
2-input NANDs = 60%
Average fanout = 1.7
# of outputs = 67
# of flip-flops = 17,003
3-input NANDs = 40%
Figure 2: Fault-tolerance methodology - Insertion of more barriers

Answer the following:

(a) Estimate the number of transistors in the circuit.

**Answer:**

This can be determined pretty much exactly. Let us assume that each 2-input NAND is realized using 4 transistors and each 3-input NAND is realized using 6 transistors. Further, assume that a FF requires 36 transistors (this will be the count if we realizes an edge trigger D-FF using cross-coupled two input NANDs). The total transistor count is

$$350075(0.6 \times 4 + 0.4 \times 6) + 17003 \times 36 = 2292468$$

Thus about 2.3 million transistors.

(b) Estimate the number of lines in the circuit.

**Answer:**

Using the count of 2 and 3 input gates we can determine the total number of input nets to all gates are $350,075 \times (0.6 \times 2 + 0.4 \times 3) = 840,180$.

In this counts not all outputs are counted. Note that a gate which has only one fanout is counted in this. Thus we need to determine those output lines which are not counted about. We can do that using information about average fanout. The outputs that will create additional lines are $350,075 \times 0.7 = 245,053$.
Number of inputs, outputs and flip-flop do not contribute much in this simple count.
Hence the total number of lines in the circuit is approximately 1,085,000.

(c) Estimate the number of two line bridging faults in the circuit.

**Answer:**

With about a Million lines in the circuit the number of two line bridges will be about square of the number of lines, hence $10^{12}$ faults.

(d) Estimate the number of gate delay faults in the circuit.

**Answer:**

This will be same as the number of gates in the circuit, i.e. 350K faults.

7. **(15 points) Fault modeling (HW)**

Circuit modification by adding more logic and inputs to a circuit, can be used to model various other faults by a single stuck-at fault model in a circuit. However, it is also possible to model other faults by adding more logic and no extra inputs in most cases. Note it is important that the circuit should have simultaneous capability to work as a fault free circuit with fault of interest. Now consider the circuit shown in Figure 3

![Figure 3: A circuit with fault candidates](image-url)
(a) Draw a modified version of the circuit that can be used to model two simultaneous stuck-at-1 faults as shown in the circuit by a single stuck-at fault in the modified version of the circuit.

**Answer:**

See the Figure 4
(b) Draw a modified version of the circuit that can be used to model a 1-dominant bridging fault (OR type of bridge) between a pair of lines X and Y marked in the circuit.

**Answer:**

See the Figure 5

![Figure 5: A circuit to model bridge line fault](image-url)

8. **(10 points)** Hadzilacos and Toueg [null:93] list four fault/failure classifications used to model faults in distributed systems.

**Answer:**

i) crash failure

ii) omission failure

iii) timing failure

iv) arbitrary or Byzantine failure

(a) Determine a relation between these models in terms of which is most general, most restrictive and how these are contained in one another.

**Answer:**

See Figure ??.
(b) Now consider an *incorrect computation fault* and determine if it can be identified to be in one of these classes or does it require a modification/addition to the above classification.

**Answer:**
See Figure ??.

9. (10 points) Refresh your probability background.

Using a simple example show the following:

**Answer:**

Let us consider casting of a die.
Let $A$ be the event of getting a 1
Let $B$ be the event that the value is odd
Now $P(A) = 1/6$
$P(B) = 3/6 = 1/2$
$P(A/B) = 1/3$
$P(A \cap B) = 1/6$

(a) $\text{Prob}(A/B) \neq P(A)$ **Answer:**

$1/3 \neq 1/6$

(b) $\text{Prob}(A/B) \neq P(B)$ **Answer:**

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\[ \frac{1}{3} \neq \frac{1}{2} \]

(c) What is the relation between \( \text{Prob}(A/B) \), \( P(A) \), \( P(B) \), \( P(A \cap B) \) and use your example to demonstrate the relation. **Answer:**

\[
P(A/B) = \frac{P(A \cap B)}{P(B)}
\]