On-Chip Reliability Monitor for Measuring Frequency Degradation

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ABSTRACT
In the aging tolerant digital circuit design, precise measurement of digital circuit degradation is a kind of key aspect. In this project, we will build a type of digital on-chip reliability monitor for measuring degradation of frequency in high-resolution for digital circuits. This technique is made by measuring the beat frequency of two ring oscillators, which has one stressed and another unstressed for reference, to get the sensing resolution which is 50 times higher than the conventional methods. In our design, we are using the 1 V, 32 nm CMOS technology to build this frequency degradation monitor scheme.

INTRODUCTION
As the CMOS process technology currently growing in the scale, it is becoming more difficult to design the reliable circuit while dealing with each node. Different kinds of reliability problems, such as TDB (time-dependent dielectric breakdown), BTI (bias temperature instability), HCI (hot carrier injection) is happening more frequently than before in the CMOS devices. NBTI (negative bias temperature instability) is one of the most pressing of these challenges.[1]-[4] It is resulted from the trap generation in the pMOS transistors’ Si-SiO2 interface, whose structural mismatch caused the dangling bonds. The dangling Si bonds will be changed to the Si-H bonds, which are easier to break when using the device, leading to the H atoms becoming gate oxide and broken bonds becoming traps, which caused the driving current of pMOS transistors getting lower. When the device is stressed, the value of the threshold voltage Vtp is increasing in its absolute value (|Vtp|), which indicates the NBTI effect. When the stress condition is removed (Vgs=0), the device is reaching the recovery or passivation phase, causing the H atoms diffuse back towards the Si-SiO2 interface, and the broken Si-H bonds will be annealed, and thereby the value of Vtp is decreased.[5]-[11]

In order to know the NBTI effect on the circuit, we need to accurately measure the reliability of the circuit. There are some types of conventional ways to measure the reliability, such as device probing or on-chip ring-oscillator frequency monitoring, but those methods need an extensive measurement setup or have some limitations of the sensing resolution. [12][13] Furthermore, it cannot acquire statistically large number of data points in different stress conditions, which is important in understanding the complexity of aging. In our project, we will build an on-chip reliability monitor which can improve the sensing resolution and monitor the aging effect precisely in digital circuits, and we will use HSPICE software simulation to validate the function of our design.
DESCRIPTION OF SYSTEM MODEL

THE SCHEME OF BEAT FREQUENCY DETECTION

Our design in detecting the frequency degradation consists of two ring oscillators and one phase comparator. We will stress only one in two ring oscillators in the stress period, and the other reference oscillator is unstressed. We use the supply voltage VDD-STR and 0V respectively for the stressed and unstressed oscillators in stress period, and use VDD-REF for both of them in measurement period. The reason that the supply voltage is set to 0V for reference oscillator in stress period is that it can prevent the device from aging. The phase comparator is used to measure the beat frequency which is defined by fstress-fref, where fstress and fref are the stressed and reference oscillator frequency respectively. After each stress period, the counter will get the output value N, and the beat frequency period is the same as the duration when there is one clock difference between the number of reference and stress pulses. The beat frequency has both the equation of N/fref and (N-1)/fstress. The counter output after stress has the value N', and similarly the beat frequency after stress can be defined as N'/fref and (N'-1)/fstress. We can derive the frequency degradation equation (fstress-fstress)/fstress=(N'-N)/(N(N-1)). The advantage of this measurement is that it can achieve a high sensing resolution when there is only small frequency degradation. From fig.2, we can see that when there is only 1% frequency degradation, the counter output N will decrease by almost half of the total value. As for the previous techniques, only a single ring oscillator is used, so it cannot make comparison between the already stressed ring oscillator and the intact reference ring oscillator, and 1% degradation in ring oscillator frequency will only cause 1% change in counter output. [9] Frequency degradation which is caused by device aging is usually less than 10% [9], so we can use almost 90% of the code to detect the 10% change in frequency. By seeing the equation in fig.2(b), we can find that if the initial counter output value N is becoming larger, the sensing resolution will also increase.

2. ARCHITECTURE OF SILICON ODOMETER TEST CHIP

Figure 3 gives us an illustration of the silicon odometer test chip architecture. The two ring oscillators are using the identical structures which both have 105-stages, but they have different inputs. Because the output of these two ring oscillators serve as the differential input of phase comparators, the Process-Voltage-Temperature (PVT) variations that affect both ring oscillators equally will be cancelled out. The phase comparator will generate the signal which shows the difference between the frequencies of stressed and reference ring oscillators, and some bubbles may appear in the output of phase comparator because of jitter effect, and it can be erased through the 5-bit majority voting circuit. The beat frequency detector will detect the pulse coming from the 5-bit majority voting circuit, and produce a DETECT signal, which will be sent to the
counter to get the output, and sent to the register to reset the counter for the next measure cycle. The measured counter outputs will be used for calculating the frequency degradation.

3. RING OSCILLATOR

![Fig.4. Ring oscillator circuit and ROSC switched-capacitance stage module](image)

The schematic of the ring oscillator is shown in figure 4. There is a virtual VDD which has multiple voltage options to choose. In the stress period, the stressed ring oscillator will change its VDD into VDD-STRESS, and the reference ring oscillator will connect its VDD to 0V in order to remove the stress. When in measurement period, the virtual VDD port of both ring oscillators will be connected to the VDD_NOM. We can measure the degradation induced by NBTI by measuring the two different measurement periods. Stress mode control 1 can be used to apply DC or AC inputs, or it can be used to toggle the ring oscillator input in each stress period to measure the circuit recovery with stress in different inverter stages. Stress mode control 2 can be used to disconnect the ring oscillator and change to stress modes. The ROSC frequency trimming module is used to adjust the initial frequencies of ring oscillator, because the initial counter output is sensitive to mismatches between two ring oscillators.

4. PHASE COMPARATOR

![Fig.5. Phase comparator circuit module](image)

Phase comparator module is shown in Fig.5. It is a crucial part in measuring the beat frequency of two ring oscillators. A clock control signal coming from the ring oscillator signal is set as the input of CLK, which is the control of phase comparator modes. When the CLK input is 0, this circuit is in pre-charge mode, and the value of node x is set as 1. When the CLK is changed to 1, the circuit becomes the evaluation mode, the switch controlled by the negation of CLK is turned on, and the value on node X will be decided by the value of A and B, which comes from the two input signals ROSC_REF and ROSC_STRESS. When A is 0 and B is 1, the value on node X will be changed to 0, which resulted in the value on PC_OUT to be 1. When the CLK is switched to value 0 again, PC_OUT will keep its current value. The frequency of the stressed ring oscillator will decrease with the effect of aging. This will cause the decrease in the overlapped region, which means the phase comparator will continuously go to low voltage until another overlapped region occurs. We will find that the output pattern of the phase comparator will repeat again, when the difference between the two input signals is exactly one clock cycle. However, accurate measurement of phase is very difficult, because it requires very high resolution of phase comparators. The beat frequency detection scheme can solve this problem, because any of non-ideal offset just shifts the start or end point without changing the period. Because the beat frequency detection scheme used the difference of two input signals rather than direct non-differential measurement method to measure the period, beat frequency detection can easily overcome jitter problems.

5. MAJORITY VOTING CIRCUIT

When signals are closely aligned, there will be uncertainties in the phase comparator circuit that it will generate undesired output. We need to build some logic circuits to filter out the unwanted data bits.
In Figure 6(a), 11011 is such kind of undesired output because it has one 0 among a stream of 1. Using 5-bit majority voting circuit, the bubbles of the 5 data bits can be removed at the output. Another example is the 11001, when we put it into a 5-bit majority voting circuit, it will correct the errors and produce another stream of 1.

Fig.6(a) Operation of the 5-bit Majority Voting Circuit

In this section, we are going to show the result of the simulation of each module. The simulation is made on the HSpice software.

Ring Oscillator Circuit:
The simulation result of our implemented ring oscillator is shown above. We can input different control signals to generate different frequency with respect to different stress or measurement situation. In order to fine tune our ring oscillator outputs, we have added a frequency trimming circuit with linear binary control code in every stage of ring oscillator.

Phase Comparator Circuit:

The simulation result of phase comparator circuit is shown above. When the clock is 0, the PC_OUT is kept the same value as previous clock. When the clock is 1, A and B will evaluate the value of PC_OUT. The PC_OUT will become high only if both A’ and B are high.

Majority Voting Circuit:

The simulation result of our implemented majority voting circuit is shown above. When the output of phase comparator PC_OUT is sent to the majority voting circuit, the majority voting circuit will remove the undesired data bit 0 in the data stream and achieve the output of majority voting circuit VOTE_OUT as a continuous data stream of 1’s.

Beat Frequency Detector:

The simulation result of beat frequency detector circuit is shown above. The majority voting circuit will output the continuous stream of 1’s (VOUT_OUT), and VOUT_OUT is sent to the beat frequency detector to find the beat frequency. The detector will detect the rising edge of VOUT_OUT and produce the beat frequency output at V(Detect).

Counter:
The simulation result of the 8 bit counter circuit is shown above. This counter consists of 8 DFF to build a series of mod 2 circuit.

Total circuit:

The simulation result of the total circuit is shown above. From seeing this simulation waveform, we can validate that this entire model works well.

COMPARISON AMONG EXISTING SCHEMES

Besides NBTI, there are some other types of effect such as HCI, RTN, TDDB, they will cause the fluctuation of the threshold voltage, thus result in the change of the frequency of the system. HCI effect is caused by the hot electrons tunneling through the oxide gate and show up as gate current or the leakage current. TDDB effect will lead to the degradation of drain current and shift in threshold voltage. RTN effect will lead to the huge fluctuation of threshold voltage, thus causing the read operation error and the device instability.

Except for the schemes of measuring NBTI effect, there are also schemes to handle these other types of effects describe above. The team of Chris. H. Kim changed the ring oscillator architecture and developed an all-in-one silicon odometer for separately monitoring HCI, BTI and TDDB. Then, by estimating the percentage change in rising and falling edge of duty cycle of the clock, the team of Chris. H. Kim used the odometer to measure the statistical behavior of NBTI and RTN on logic circuit. Later, the team of Chris. H. Kim built the odometer to measure the impact of interconnect wire length on BTI and HCI aging. And the team of Wei Hwang and Shyh-Jye Jou presented an embedded SRAM oscillator for in-situ measurement of frequency degradation. What is similar is that they are all using the way of measuring the frequency to observe how severe the threshold voltage has been changed.

CONCLUSION

Considering the reliability and circuit performance, NBTI effect is causing an impact in the aging of the circuit. Sometimes we need to monitor the subtle change in the aging of the circuit while using the circuit. We have done the software simulation of NBTI monitoring circuit that has the function of detecting the aging effect in a precise way. This monitoring scheme is based on the beat frequency detection of two ring oscillators, which has a much higher sensing resolution than the conventional schemes. This approach of measurement can also minimize the effect of the Process-Voltage-Temperature variations.

The relationship between true inverter chain and ring oscillator frequency degradation is analyzed in both DC and AC stress conditions. We have used the 1volt 32 nm technology file to build the On-Chip reliability monitor for measuring frequency degradation. We have validated that when there is a 30mV change in pMOS threshold voltage, our design can detect a 3.3% degradation in ring oscillator frequency.
REFERENCES


