ECE 753: FAULT-TOLERANT COMPUTING

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Fault Modeling
Lectures Set 2

Overview

- Fault Modeling
- References
- Introduction
- Fault models at different levels (HW)
- Error models
- High-level failure models (process or system failure)
- Summary

Recap

- Think about PROJECT
- Terminology and definitions
- Fundamental principles - Redundancy
  - Hardware - low and high level
  - Software
  - Time
  - Information
- FEF Chain and methods to break it (barriers)
  - Attributes of faults and fault types - such as permanent, transient, intermittent (please read)

Fault Modeling

References

- [mull:93] Hadzilacos and Toueg, Fault tolerant broadcast and related problems, in Distributed systems (book)

Fault Modeling (contd.)

Introduction

- What is a model?
  - An abstraction that captures the behavior of the original system.
  - must be simple
  - must lead to accurate conclusions

Fault Modeling (contd.)

Introduction

- Why use a model?
  - tractability of analysis
  - a non-destructive method to study (low cost, alternative to fault injection)
  - manageable study space (can check equivalence and reduce the study space)
Fault Modeling (contd.)

Introduction

- Different models at different levels of abstractions:
  - Chip level - manufacturing defects, random faults, transistor faults, gate failures, aging, ...
  - System level
    - HW - aging, interconnect failures, chip failures, ...
    - SW - bugs, design flaws, incorrect algorithms, ...

Fault Modeling (contd.)

Fault models at different levels (HW)

- Process level
- Transistor level
- Gate level
- Function level (often error models)
- Behaviour level (often timing failure models)
  - System level (usually failure models)

Fault Modeling (contd.)

Fault models at different levels (contd.)

- Process level - Defect models
  - cluster defects
  - point and random defects
  - used to predict the process yield
  - tested using optical and parametric tests
  - effect of defect
    - chip fails to perform its function
    - unacceptable parameters - large capacitance, large delay, slow speed, high current

Fault Modeling (contd.)

Fault models at different levels (contd.)

- Transistor level - failure of a transistor
  - fabrication level causes - point defects, mask misalignment, design rule violation
  - physical facts - shorts, opens, line-bridges,
  - others
    - size variations -> altered delays
    - coupling/crosstalk
    - degradation of elements - electromigration
    - alpha particle hits
    - power transients
    - missing/extra transistors – PLAs
    - Function modification/alteration - FPGA

Fault Modeling (contd.)

Fault models at different levels (contd.)

- Transistor level - erroneous behaviors
  - High current
  - incorrect logic output
  - intermediate voltage
  - different performance (operating speed)
  - state change - alpha particle hit

Fault Modeling (contd.)

Fault models at different levels (contd.)

- Transistor level - prevalent fault models
  - stuck-on and stuck-off faults
  - bridging fault
  - strength of signals
  - delay fault
  - coupling and cross talk

- Limitations
  - very large number of possible faults makes it difficult to handle these faults (intractability due to large model space)
Fault Modeling (contd.)

Fault models at different levels (contd.)

- Transistor level - comments (these are fairly general and are not restricted to transistor level model)
  - increasing computing power implies that we can handle large number of faults and complex models
  - these models used for test generation and not for fault tolerance per say
  - methods have been proposed to reduce the number of faults that need to be studied - e.g. fault equivalence
  - classical method and newer methods (such as current testing) are employed in real testing
  - design for testability and built-in self-test are becoming prevalent

Fault Modeling (contd.)

Fault models at different levels (contd.)

- Gate level - causes
  - same as for transistors
  - additional causes in SSI and board level - failed resistor, failed solder joint, failed wire wrap, …
- Gate level - erroneous behaviors
  - similar to those as for transistors

(one of the most commonly used model - why? See next slides)

Fault Modeling (contd.)

Fault models a different levels (contd.)

- Gate level - different models
  - Stuck-at: a line value stays the same irrespective of the signal applied to the line
  - Advantages
    - simplicity
    - accuracy
    - can model most real faults
    - tractable model space - count the possible number of faults
    - easy to use and easy to quantify (for quality metric)
    - substantial empirical evidence of its practical use

Fault Modeling (contd.)

Fault models a different levels (contd.)

- Gate level - different models
  - Stuck-at - (contd.)
    - Disadvantages
      - with increasing device density the model is being questioned often and losing many of its advantages
      - Some real defects can not be modeled by this model
      - more powerful computers are making it possible to handle other models - even at fabrication level

Fault Modeling (contd.)

Fault models a different levels (contd.)

- Gate level - different models
  - Bridging faults - pair of lines in a circuit (at gate level) are shorted. Many variations such as intergate, intragate, neighboring lines, …
  - Advantages
    - simple
    - realistic
  - Disadvantages
    - large number of faults
    - difficult to relate to the quality metric

Fault Modeling (contd.)

Fault models a different levels (contd.)

- Gate level - different models
  - Stuck-open/Stuck-On - Transistor based open fault can be modeled by logic level. Some time extra logic gates are used to model opens in this manner similar to modeling bridging faults
Fault Modeling (contd.)

Fault models a different levels (contd.)

- Gate level - different models
  - Delay faults - delay of a gate or a line is different than the nominal or know delay in a perfect process
  - Important paths - gate delay, path delay, ...
- Advantages
  - Performance oriented modeling
  - Quite general
- Disadvantages
  - Difficult to use and intractable (path delay)

Fault Modeling (contd.)

Fault models a different levels (contd.)

- Gate level - different models
  - Other models
    - Coupling between pair of lines
    - Pin or I/O faults in gates (or chips)
    - Speedup/slow down of signals (sub-micron technologies)
    - Aging (such as NBTI in sub-micron technologies)

Fault Modeling (contd.)

Fault models a different levels (contd.)

- Function Level - when used
  - Lower level description is not available
  - Function level processing (e.g. simulation) is often faster
  - Design available only in mixed form (gate and function)

Fault Modeling (contd.)

Fault models a different levels (contd.)

- Function Level - where used
  - Combinational circuits
  - Logic blocks
  - Decoders
  - Finite state machines
  - Large complex circuits
  - Microprocessors (often only mixed form is available, such as ALU in gate level, memory in functional level, etc.)
  - For other building blocks
    - PLAs, RAMs, FPGAs

Fault Modeling (contd.)

Fault models a different levels (contd.)

- System Level - when used
  - Interconnected systems
    - Ad hoc connected systems
    - Regular connected systems
  - Failure of a system or systems, or interconnects
    - Many failure models exist and will be discussed later in the course

Fault Modeling (contd.)

Fault models a different levels (contd.)

- Error models
  - Means of classifying the effect of physical fault(s) in a system - note from modeling point of view it is not necessary that we deduce it using a fault model
  - Goals
    - Extent of information corrupted
    - Extent of error(s) propagated
    - Latency issue
Fault Modeling (contd.)

Error models (contd.)

- Error effects
  - data
  - control
  - state

- Error Types (HW)
  - bit errors (data, control, state) - single bit error
    assumption commonly used in practice
  - unidirectional errors (mostly in data)
  - byte errors (data)
  - other - intermediate logic level

Fault Modeling (contd.)

Error models (contd.)

- Error Types (SW)
  - branch error
  - missing instruction error
  - missing/dangling pointer errors

Fault Modeling (contd.)

High-level failure models (process or system failure)

- System model
  - single or multiple processor system
  - single - multiple processes executing
  - key - interacting processes - such as message passing systems, distributed systems, ...

Fault Modeling (contd.)

High-level failure models (process or system failure)

- General classification
  - crash failure - a faulty processor or system stops permanently
  - omission failure - a faulty process omits inputs/outputs some times but when it works, it works correctly
  - timing failure - inputs/outputs are delayed or arrive too early
  - Byzantine failure or arbitrary failure - a faulty processor can exhibit arbitrary behavior including malicious nature

Summary

- Fault modeling
  - References
  - Fault models at different levels
  - Error models
  - Process or system failure models