

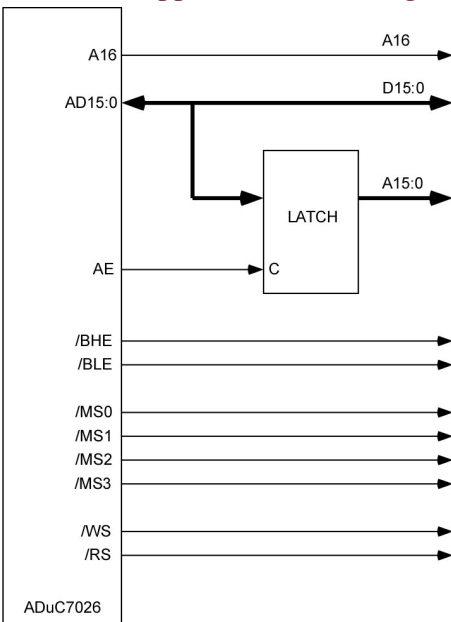
**HOMEWORK ASSIGNMENT #5**

Due Friday April 10th, 2009

**1. (20 points) Extending Memory Depth and/or Width**

Find the datasheet for a Cypress Semiconductor CY7C1399BN. Using 2 of these devices, you will design a 64KB memory bank for use with the **ADuC7026**'s external memory interface. The memory bank is to be designed with a 16-bit width, and to support byte read/write capability.

Show all required connections to the SRAM devices, and how the system will connect to the ADuC7026 external memory interface. Use NANDs, NORs, Inverters as needed. Assume that a demultiplexed bus is already available in the system, as shown in the figure below. The memory should be mapped to the MS0 region. Points will be deducted for a messy schematic.

**2. (25 points) ADuC7026 Timing Analysis**

Now, analyze the memory system that you designed in problems #1. Assume that the propagation delays are as follows: latch (from any input) - 10ns, gates (NANDs, NORs, Inverters) (from any input) - 5ns. The ADuC7026 is assumed to be running with a CPU core clock of (1275 x 32.768kHz) at 3.3V. You are to determine if the CY7C1399BN device is compatible with the ADuC7026 external memory interface. Evaluate the read & write timing to determine if the SRAM is compatible with the ADuC7026 system. To do this, verify that all the timing requirements for both the ADuC7026 (is data driven in time and held long enough, and are there any contention issues) and the SRAM are met (there are 3 timing variants available use the 20ns access time data set). Determine what if any wait states are required, and tell the values you would program into the XMxPAR register.

For the ADuC7026, assume that  $t_{\text{DATA\_SETUP}} = 10\text{ns}$  and  $t_{\text{DATA\_HOLD}} = 0\text{ns}$ . Use the timing relationships given on the in-class handout, not those on the ADuC7026 datasheet timing diagram.

**3. (10 points) Memory Types. (fill in this table) (handwritten is fine)**

| Memory Type: | Description: | Describe application it is suited for |
|--------------|--------------|---------------------------------------|
| ROM          |              |                                       |
| SRAM         |              |                                       |
| Flash        |              |                                       |
| DRAM         |              |                                       |
| Cache        |              |                                       |

**4. (10 points) Memory Nuances**

Explain the differences between the following 4 memories in the non-volatile family (Flash, EEPROM, EPROM, and OTP).

Explain the difference between via programmed and diffusion programmed ROM. What are advantages/disadvantage of each.

Imagine a 2-way set associative cache memory for an ARM processor (32-bit addressing). Each way contains 4k entries of 32-bit words. How many bits wide would the tag portion of the array need to be? Show how you derived this & sketch out the basic structure.

**5. (10 points) EEPROM Memory System Usage**

A. Erasing an EEPROM cells is a destructive process, and so EEPROMs have limited endurance. Suppose that you use the 128kB AT28LV010 EEPROM memory subsystem in a product that needs to maintain some information in non-volatile memory, and that the information is updated once per second. Assume that you need to store 120 bytes of information at a time. Nothing else needs to be stored in the EEPROMs. Describe how you could use the 128kB EEPROM memory system to store this information so as to maximize the length of time the system could be expected to operate correctly. How long would the system be guaranteed to operate correctly? You cannot assume that the product will be left on continuously. **Note:** obviously you are going to distribute the 120 bytes over the 128kB memory to distribute wear evenly. The challenge here is to think of an addressing mechanism to know which block contains the current valid set of data.

**6. (15 points) Building Programming Proficiency**

Implement a bubble sort algorithm in a subroutine *bsearch*. The subroutine will be passed the starting address of an array of unsigned words in R0, and the unsigned length of the array in R1. The length of the array may be any value, including 0. The array should be sorted in ascending order. Ensure that *bsearch* is exported from the file. Do not corrupt any of the caller's registers. We will test your subroutine by linking it with a driver program.

**Important:** Submit ONLY your program source code file *teamX\_bsearch.s* using the homework 5 dropbox in Learn@UW. Also, submit a **paper copy** of *teamX\_bsearch.s* with the rest of the assignment.

**7. (10 points) Quiz Question**

Design one original quiz question operating at Bloom's Taxonomy level 3 for any material covered in Module 5. This must test one of the module objectives in a specific problem. Explicitly state which particular objective you are attempting to test. Provide a complete, detailed solution to your question.